Federal Agencies
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Audio Analog-to-Digital Converter Performance Specification and Test Method

Introduction

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The FADGI Audio-Visual Working Group
http://www.digitizationguidelines.gov/audio-visual/

Audio Analog-to-Digital Converter
Performance Specification and Test Method

Introduction

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Scope

This document provides an explanatory background to the Federal Agencies Digital Guidelines Initiative (FADGI)[1] recommendation for metrics and methods pertaining to the performance of audio analog-to-digital converters (ADCs) in preservation reformatting workflows. The guideline recommendations and this explanatory document are products of FADGI's Audio-Visual Working Group.

This introduction is one of four related documents pertaining to system performance. The companion documents are:

- *Guideline for Audio Analog-to-Digital Converter Performance Specification and Test Method* (August 2012)
  - http://www.digitizationguidelines.gov/audio-visual/documents/ADC_performGuide_20120820.pdf
- *Assess Audio System Evaluation Tools: Consultant's Initial Report* (March 2011)
  - http://www.digitizationguidelines.gov/audio-visual/documents/FADGI_Audio_EvalPerf_Report.pdf
- Previous draft of the introductory discussion and performance guideline (February 2012)
  - http://www.digitizationguidelines.gov/audio-visual/documents/ADC_Perf_Test_2012-02-24.pdf

The Working Group's expert consultant Chris Lacinak (Audiovisual Preservation Solutions) was the principal investigator and main author for all of these documents. During their development, Lacinak received valuable guidance from a number of members of the Working Group and from outside experts, notably Richard Cabot[2] and Ian Dennis.[3]

The performance of the systems used to digitize sound recordings is multifaceted, including the following elements:

- The performance of the analog-to-digital converters (ADCs), the topic of this introductory document and the guideline it accompanies.
- Flaws in a recording caused by interstitial errors, where samples are dropped or otherwise altered in the final digital audio file when it is written to media. Interstitial errors and their identification are the topics of a separate still-in-process report for the Working Group by Audiovisual Preservation Solutions.
- The selection and placement of other devices, cables, or interfaces in the signal chain. This topic is beyond our scope at this time.

This introduction explores three aspects of ADC performance: (1) which parameters or features warrant measurement in the first place, (2) what performance specifications are appropriate for high quality content in an archival context and (3) what methods ought to be used to make the measurements?

Readers should note that the Working Group's scope does *not* include the intricacies of the playback of historical materials such as discs, tapes, and cylinder recordings. In addition, this

[1] http://www.digitizationguidelines.gov/

[2] Richard C. Cabot has a Ph.D. from Rensselaer Polytechnic Institute and his professional career has included work at Tektronix, Audio Precision (which he co-founded), XFRM, Inc., and Qualis Audio. Cabot also chairs the committee that developed the AES-17 digital audio measurement standard.

[3] Ian Dennis is the co-founder and Chief Technical Officer at Prism Sound, a well-known manufacturer of digital audio systems.

activity does not cover the performance of systems used to create new recordings in the studio or in the field. It is the case, however, that many of the issues and metrics under discussion here are not limited to preservation reformatting and apply equally to the performance of systems used to create of new recordings.

Sources of Information and Inspiration

There are two critical starting points for this study. The first is an excellent listing of parameters and performance specifications is provided in *TC 04: Guidelines on the Production and Preservation of Digital Objects, 2nd ed., 2009*,[4] published by the International Association of Sound and Audiovisual Archives (IASA). Although this report recommends some adjustments to TC-04, it is still the case that the preservation community owes a great debt to this important work. The second starting point is a pair of standards that provide a rich source of information on methods. One is *AES17-1998 (r2009): AES standard method for digital audio engineering — Measurement of digital audio equipment (Revision of AES17-1991)* from the Audio Engineering Society (AES) Standards Working Group SC-02-01 (Digital Audio Measurement Techniques).[5] The other is *IEC-61606-3 Audio and audiovisual equipment - Digital audio parts - Basic measurement methods of audio characteristics - Part 3: Professional use* (2008) from the International Electrotechnical Commission (IEC) technical committee 100 (Audio, video and multimedia systems and equipment).[6] Chris Lacinak, the main author of the FADGI guideline and this introduction, is a member of the Audio Engineering Society standards working group SC-02-01, currently undertaking a revision of AES17. The process of developing the FADGI guideline and this introduction has been informed by both the published standards and by ongoing discussions concerning proposed revisions to AES17.

Levels of Device Performance

The metrics specified in the guideline pertain to the production of files using the highest quality ADC devices. Comments from within and without the Working Group, however, have called attention to the range of types of archival organizations, some with strong resources and others in modest circumstances. Commentators have also noted the variation in the categories of material to be reformatted, asking if there might be circumstances in which relaxed levels of device performance would be acceptable. The Working Group hopes to address this topic in the near future.[7]

Is Initial Testing and Continuing Monitoring Necessary?

As the FADGI Working Group began to plan the development of this guideline, and as the principal investigator talked to other specialists, there was some discussion of the need for device performance testing. Some individuals noted that ADC manufacturers generally publish specifications for their equipment and questioned the need for initial testing. Others questioned

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[4] Web version and pdf download available at http://www.iasa-web.org/tc04/audio-preservation
[5] http://www.aes.org/publications/standards/search.cfm?docID=21
[6] http://webstore.iec.ch/webstore/webstore.nsf/artnum/041968!opendocument
[7] In a parallel effort by the Federal Agencies Still Image Working Group, four performance levels have been associated with the same set of target specifications. All levels have the same "aim points," but they allow for varying tolerances, i.e., the highest performance level allows very little variation from the target value while the lowest performance level allows for a much greater level of variation.

the need for routine and ongoing testing, noting that very often the failure of a device is very obvious. This writer and Working Group feel that initial and continuing testing are warranted for the reasons stated below.

In the initial March 2011 study (cited above), the principal investigator looked at examples of the specifications published by ADC manufacturers, noting that these often fail to provide complete statements of what has been measured or about the test methods employed, inhibiting easy comparison of ADCs in the marketplace. Next, he downloaded published specifications for several ADCs and compared them to the IASA TC-04 performance specifications. In some cases, the published specification omitted elements listed in TC-04 while in other cases, the delineation of the manufacturer's specification made it challenging to compare to the IASA pass-fail requirements. In many cases, manufacturers did not report on the test method used to produce the values provided, adding to the challenge in performing a comparison.

The March 2011 study also considered the need to test an ADC an ongoing basis, especially since some specialists feel that the failure modes of current high quality ADCs render costly routine testing and measurement unnecessary. Constraints of time, however, prevented any systematic study of failure modes. Nevertheless, the principal investigator carried out a series of informal conversations with experts in the field, including the attendees at a meeting of the AES committee on Digital Audio Measurement Techniques. The responses, although anecdotal, were very consistent. All of the experts consulted favored routine testing, arguing that ADCs are no different than any other type of equipment and stating that these devices can fail in nuanced and subtle ways, on both analog input and digital output. In effect, the stance reflected the engineers' historical stance regarding equipment of all types, i.e., that standard operating procedure in professional audio studio environments includes testing the performance and integrity of equipment and signal paths on a regular and ongoing basis.

Framing the Analysis

The general thrust of this performance study is *how* and *what* to measure, and the determination of *acceptable results*. In order to frame the text that follows, these elements have been recast as follows:

- Are the IASA performance specifications set at the appropriate level of stringency for a standard representing the highest level of required performance for preservation purposes?
- Are the number and types of tests being performed sufficient and appropriate to assess the quality of an ADC for preservation purposes?
- For any new test methods proposed for inclusion in the core test suite that do not have IASA performance specification counterparts, what is the recommended performance specification?

The principal investigator sought feedback on these questions from ADC manufacturers, test and measurement companies, and the Audio Engineering Society standards committee on Digital Audio Measurement Techniques. Although everyone shared an interest in maintaining a minimal approach, the consensus indicated that the proposed IASA/AES test suite would benefit from being more comprehensive. The individuals consulted recommended a number of tests beyond those in the original IASA performance specifications, and some of these have been included here. Additional comments suggested adjusting the stringency of some of the pass-fail aim points, a suggestion that was reinforced by the field testing described in the next section. As

is noted in *Field Test Summary and Conclusions* (pages 27-28), the Working Group posted the guideline and introduction for public comment from February through July 2012. The comments received did not suggest specific changes to the metrics but they called for improved explanations in this introduction and in the guideline itself, as well as noting some topics that warrant future exploration.

Testing to Refine the Metrics

As the modified test suite and performance specifications were being drafted, a set of field tests were devised. These consisted of carrying out performance tests on five ADC devices, including examples of converters currently used by various federal agencies and covering a range of price points and published technical specifications. This was not intended to be a test of these devices per se, but rather a way to assess the efficacy of various metrics and methods. Only one instance of each device was tested. In contrast, a device-evaluation activity would test and compare multiple instances of each device in order to compensate for the presence of sample-specific defects. Since this field test was not a device test, this report does not identify the devices.

The converters offered different combinations of output formats, input-limiting circuitry, dithering processes, and number of channels. Although four of the five units included digital-to-analog converters (DAC), this was not considered in scope for this study and was not evaluated. Two of the five units were multichannel devices and the other three were two-channel devices. Testing was limited to two channels of each device.[8] Where multiple choices of dither were available, the testing was limited to flat spectrum triangular dither. These simplifications were made for schedule reasons and to ensure units were compared under similar conditions.

Following testing, the results were analyzed relative to each other and to the originating performance specifications. The resulting findings and recommendations are discussed in detail in the section titled "Device Field Testing and Specification Refinement," later in this document. In several cases the stated performance metrics were determined based on a combination of what seemed both reasonable and stringent, guided by analysis of the test results and discussion amongst test and measurement experts in the field on where to draw the line.

As with any guideline or standard, adoption and implementation over time will yield valuable feedback on further refinement of this test method and the associated performance metrics. The Working Group intends to further vet this guideline through continued efforts even as it looks to the larger community concerned with audio test and measurement to provide relevant feedback and to help advance practices and the availability of tools.

[8] Except in one instance where we determined that the performance of the front panel and rear panel line level inputs differed significantly, warranting assessment and reporting of both.

The Test Suite

General Comments about Measurement

Many measurements in this suite follow the techniques specified in AES-17 and are cited as such. The procedures in AES-17 apply to analog-to-digital, digital-to-analog, and digital-to-digital devices. As this study is primarily focused on ADCs, in many cases the procedures may be simplified. Modifications to the referenced standards are noted where applicable.

A reference level of +18 dBu was chosen as the analog equivalent of digital full scale. This is a common reference level in modern studios and broadcast facilities. Initial measurements on the converters verified that this was usable for all units.[9] Each converter's gain was adjusted to make a +18 dBu input result in 0 dBFS out.

The descriptions that follow are included to facilitate understanding of the test results. They are concise and written in a descriptive style rather than in the requirements style used in standards. The following test suite represents the tests performed as part of the study and is not the recommended final test suite. The final recommended test suite is provided in the guideline document proper.

Frequency Response

Frequency response assesses the constancy of gain across frequency, demonstrating the converters' ability to capture the signal without "coloring" its sound. For converters this is generally a flat line across most of the audio band, deviating only at very low and very high frequencies.

The measurement is performed with a variable frequency sinewave input and an rms amplitude measurement at the output. The sinewave frequency is swept from 10 Hz to 50 kHz using 10 steps per octave. The sinewave amplitude is 20 dB below full scale to allow margin for non-flat converter response without clipping the output and to reduce the chance of nonlinear behavior at the frequency extremes.

This is the procedure specified in AES-17. The measurement is performed at both 48 kHz and 96 kHz sample rates.

Total Harmonic Distortion plus Noise (THD+N)

THD+N is a basic test of converter distortion and is used to assess the amount of "junk" added to a clean audio signal. Since the measurement depends on quantifying the harmonics added to a clean sinewave it is of limited utility at high frequencies where the limited bandwidth of the digital audio format may prevent the harmonics from appearing in the output.

[9] This was later discovered to be sub-optimal for the device as discussed below. Additional measurements were made on the device unit as a result.

The ADC is driven with a low distortion sine wave. The digital output is passed through a notch filter, bandwidth limited from 20 Hz to 20 kHz and the RMS amplitude measured. The THD+N is the ratio of this value to the RMS amplitude of the unfiltered signal. The measurement is performed at all combinations of the amplitudes -1.0 dBFS, -10 dBFS, -20 dBFS and -60 dBFS and frequencies of 41 Hz, 997 Hz and 6597 Hz. The upper frequency is chosen to allow both 2nd and 3rd harmonics to pass through a 20 kHz bandwidth limited digital interface.

This procedure follows the AES-17 standard, differing only in the frequency and level combinations employed. The measurement is performed at both 48 kHz and 96 kHz sample rates.

Dynamic Range/Signal to Noise Ratio

Dynamic range is an approximation to the perceived noise in the converter, giving an indication of the widest dynamic range which may be accommodated when using the converter.

The ADC is driven with a low amplitude, mid frequency sine wave (-60 dBFS, 997 Hz). This ensures that the converter is active rather than producing a static digital output value. The sinewave is removed from the output using a digital notch filter resulting in a signal representative of the noise generated by the converter. This is passed through a weighting filter (A-weighting, band limited to 20 kHz, for these measurements) to simulate the ears sensitivity at low levels. The rms amplitude is measured and expressed in dB relative to full scale (dBFS).

This differs from AES-17 in that A-weighting is used in place of CCIR weighting. Measurements are also made unweighted, with a 20 Hz to 20 kHz bandwidth limit. Both are reported for each channel, giving a total of 4 measurements.

Intermodulation Distortion

The AES-17 test method provides the option of performing a Low Frequency (LF) test and a High Frequency (HF) test for *Intermodulation Distortion (IMD).*

High Frequency Intermodulation Distortion

High frequency intermodulation distortion (HF IMD) is an alternative test of converter distortion. By using two closely spaced high frequency sinewaves and measuring the modulation they induce on each other it is possible to measure nonlinearities at frequencies close to the high frequency bandwidth limit of the converter.

The converter is driven with two equal amplitude high frequency sinewaves (18 kHz and 20 kHz) whose combined peak-peak amplitude reaches 1 dB below the full scale input amplitude. The full output spectrum is provided graphically. The sum of second- and third-order difference frequency components in the output are measured and reported in dBFS.

This is essentially the procedure specified in AES-17, except for a 1 dB reduction in signal level. The AES-17 directive to perform IMD measurements at full scale is

dangerous in that clipping can occur with minor changes in level resulting in unfairly elevated distortion values. This is avoided by using the -1 dBFS level specified here.

Low Frequency Intermodulation Distortion

Low frequency intermodulation distortion (LF IMD) is another test of converter distortion or the amount of "junk" added to a clean audio signal. It uses two widely spaced sinewaves, one high frequency and one low frequency. The modulation induced on the high one by the low one is measured. As with the high frequency intermodulation measurement it is possible to assess nonlinearities at frequencies close to the high frequency bandwidth limit of the converter. Unlike the other test, this looks for low frequency converter limitations as can occur with inadequately stiff reference voltage regulation and filtering.

The converter is driven with two sinewaves, one low frequency (41 kHz) and one high frequency (7993 Hz). The low frequency sine amplitude is 4 times that of the high frequency sine and their combined peak-peak amplitude reaches 1 dB below the full the scale input amplitude. The output spectrum is provided graphically. The sum of second- and third-order difference frequency components in the output are measured and reported in dBFS.

This is essentially the procedure specified in AES-17, except for a 1 dB reduction in signal level. The AES-17 directive to perform IMD measurements at full scale is dangerous in that clipping can occur with minor changes in level resulting in unfairly elevated distortion values. This is avoided by using the –1 dBFS level specified here.

Amplitude Linearity

An amplitude linearity test examines the behavior of converters with varying input signal level. It is particularly sensitive to modulation of the background noise by the input signal and in showing inconsistent quantization behavior.

Called level-dependent logarithmic gain in AES-17, this measurement stimulates the converter with a 997 Hz sinewave of varying amplitude. The amplitude of the output sinewave is measured using a narrow bandpass filter to exclude noise, harmonics and spurious tones. The sinewave amplitude is swept from -5 dBFS to -115 dBFS and the deviation in the measured amplitude from the expected amplitude is determined. The linearity measurement differs from AES-17 in that the range is fixed, not dependent on the noise floor. This simplifies comparisons between converters. The result is expressed as a graph of this deviation as a function of input amplitude. In addition to this, the result should be expressed as a standard deviation value.

Spurious Aharmonic Signals

This measurement of spurious aharmonic signals looks at all components created in the output of the converter. The unit being tested is driven with a low distortion 997 Hz sinewave at -1 dBFS. The output spectrum is measured with a 32,768 point FFT. The full spectrum is graphed for informational purposes. For comparison, the largest aharmonic component is reported.

Alias Suppression

Alias suppression examines the ability of a converter to reject frequencies above one half the sample rate. If these are not eliminated they will appear in the output but at frequencies very different from what they had originally. This can result in strange tones and noises within the audio band that become a permanent, improper part of the recorded signal. This can be a serious problem when recording the output of analog tape recorders that leak bias signals into their outputs or when recording signals which include ultrasonic components.

The device is stimulated with a variable frequency sine wave at -10 dBFS. Beginning at half the sample rate, the frequency is continuously increased until it reaches 200 kHz. For a 48 kHz sample rate, the frequency is swept from 24 kHz to 200 kHz. For a 96 kHz sample rate, the frequency is swept from 48 kHz to 200 kHz. The rms amplitude at the converter output, increased by 10 dB, is graphed.

The difference from AES-17 is the elimination of variable frequencies based on a specified upper band edge frequency. This simplifies comparisons across converters. By starting at one half the sample rate, the AES-17 requirement for a notch filter is eliminated and the test becomes much simpler.

Cross-Talk

This measurement of cross-talk assesses how much the various channels in a multichannel converter interfere with each other. One channel is driven and the amount of that signal appearing in the other channel outputs is measured.

One channel of the converter under test is driven with a -1 dBFS variable frequency sinewave. The output of the other channels is passed through a narrow bandpass filter to assess its level, even close to the noise floor. This amplitude is expressed in dB relative to the sinewave output on the channel being driven. The measurement is performed at 20 Hz, 1 kHz and 20 kHz.

Cross-talk requirements are highly application dependent (i.e. The stringency of cross-talk is much higher for unrelated channels than related channels).

Common-Mode Rejection Ratio (CMRR)

If a signal is applied equally to both inputs of a device so that the differential input voltage is unaffected, the output should not be affected. Voltage that is common between either of the inputs and ground is called common-mode voltage. As this common voltage is varied, the perfect differential device's output voltage should hold absolutely steady (no change in output for any arbitrary change in common-mode input). In practice, however, changes in common mode voltage will produce changes in output; common-mode rejection ratio (CMRR) is the ratio of the common-mode gain to differential-mode gain. In simple terms, CMRR speaks to the ability of a device to reject noise and interference that is not part of the source signal. This noise and interference is typically the result of electromagnetic pickup in wiring between the source and the converter input.

The converter input is driven from a low impedance sinewave generator. The amplitude is adjusted to achieve -20 dBFS at the device output. The signal is removed, and the generator reconnected between the chassis ground and one side of the input. A 10 Ohm resistor is connected between this point and the other side of the input. If the input is asymmetrical, the generator is connected to the low side and the resistor to the high side. The output is measured through a bandpass filter at the sinewave frequency. The resulting rms value is reported relative to this -20 dBFS reference. The measurement is performed at 20 Hz, 1 kHz and 20 kHz.

This technique, and the 10 Ohm resistance value, corresponds to IEC 60268-3, which provides a newer method of measuring CMRR. It recognizes that rejection of interference is fundamentally limited by how a differential input deals with mismatches in the two sides of a source. Most sources are asymmetrical: balanced sources due to mismatches in the components comprising the two sides, and unbalanced sources due to the complete lack of source resistance on the low (or chassis) side. Previous CMRR tests tied the two halves of an input together and did not account for asymmetrical loading of the input.

Input Overload Behavior

Some converters behave erratically when their inputs are overloaded, either completely zeroing their output or swinging wildly between positive and negative full scale. This test quantifies the management of overloading by gradually increasing input level and looking at the distortion at the converters output.

The converter is driven with a low distortion sine wave whose amplitude is adjusted to yield -1 dBFS at the converter output. The amplitude is increased by 6 dB in 1 dB steps. The sine wave present in the output is removed with a notch filter and the rms amplitude of the remainder is measured.

This is the same basic approach used in AES-17 but finer amplitude steps are used to record more detail.

Clock and Jitter Test Methods and Metrics

Jitter is defined and described in an Audio Engineering Society Information Document pertaining to digital audio measurements, revised in 2011: *Jitter Performance Specifications*, AES-12id-2006 (r2011).[10] The introduction to this document begins with this statement: "Clocks tick at the heart of every digital audio product. Jitter on clocks that are applied to audio converters (analog-to-digital and digital-to-analog) can degrade audio performance." The document defines jitter as "the dynamic deviation of event instants in a stream or signal from their ideal positions in time, excluding modulation components below 10 Hz."

Jitter manifests itself in two places: in the sampling process (***sampling jitter***), and in the digital interface (***interface jitter***). When an ADC is only referencing its own sampling clock, the jitter that is present is referred to as ***intrinsic jitter***. ADCs may also reference an external sampling clock via digital interface, and the jitter present at the input to the ADC is referred to as interface jitter. Depending on the severity of the interface jitter and the design of the ADC, interface jitter

[10] http://www.aes.org/publications/standards/search.cfm?docID=57

can increase sampling jitter. The passing of jitter from an interface to sampling jitter is referred to as ***jitter transfe**r*. The ability of a device to attenuate interface jitter and keep it from adding to sampling jitter is referred to as ***sync input jitter susceptibility***. The additive accrual of jitter through a chain of devices is called ***jitter accumulation*.**

TC-04 provides the following performance specifications addressing clocks and jitter:

- Internal Sample Clock Accuracy. For an A/D converter synchronized to its internal sample clock, frequency accuracy of the clock measured at the digital stream output will be better than ±25 ppm.
- External Synchronization. Where the A/D converter sample clock will be synchronized to an external reference signal, the A/D converter must react transparently to incoming sample rate variations ±0.2% of the nominal sample rate. The external synchronization circuit must reject incoming jitter so that the synchronized sample rate clock is free from artifacts and disturbances.
- Jitter. Interface jitter measured at A/D output <5 ns.

Our approach to assessing clocking and jitter takes a slightly different approach to jitter and clocking, as outlined in the following sections of this document:

- Sync Input Jitter Susceptibility
- Jitter Transfer Gain
- Sync Input Lock Range

Internal Sample Clock Accuracy was omitted based on the fact that the probability of inaccuracy to the extent of causing issues within a typical preservation setup using present-day ADCs is low. This parameter does not speak to the jitter of a clock, but rather small drifts from the sampling frequency that occur due to temperature changes and over time. Based on the quality of the converters included in this study there are no real practical implications to their sample clock accuracy specifications.

Sync Input Jitter Susceptibility

Converters which sync to an external reference signal become dependent to varying degrees on the cleanliness of that signal. This test looks at the ability of the converter to reject interference which may be present on the reference and consequently the impact of sync interface jitter on sampling jitter.

The converter input is driven with a -3 dBFS low distortion sinewave at 12 kHz. The reference input is driven with a signal whose phase is jittered with a 40 ns p-p sinewave whose frequency varies from 62.5 Hz to 8 kHz in octave steps. The output spectrum is measured at each step and the results overlaid. The measurements are repeated with a 997 Hz input to the converter.

This is equivalent to the procedure in AES-17 except that the device is assumed to be only an analog-to-digital converter. If a digital-to-analog function is included, it is not used in our testing. Measurements are made locking the converter through its reference input, not its D/A converter input. This simplification eases comparisons across the variety of devices being tested and reduces the number of permutations which would

otherwise need to be tested. AES-17 also specifies that the jitter signal "is varied from 80 Hz to 20 kHz in octave steps." The range specified here goes from 62.5Hz to 8kHz. Incrementing by octaves starting at 80 Hz does not get to 20 kHz. Also, with a 12 kHz tone, sidebands from a 10 kHz modulation are about as high as can be seen. Consequently the frequency range was changed to begin and end on an IEC standard octave frequency. The upper end is set to a frequency that fits within the sideband limitations of the 12 kHz tone.

Jitter Transfer Gain

Jitter transfer gain is a metric that pertains to a converter locking to an external reference. This test analyzes the amount of interface jitter that persists from the sync input through the digital output of the device. There is rarely enough effect to impact the ability of subsequent devices to lock to the resulting digital signal. However, if devices with poor jitter transfer behavior are cascaded the cumulative effect has been known to cause problems. Moreover, converter behavior in this test reveals limitations in the devices sync input design and gives insight to its ability to properly function in a more complex digital signal chain.

The reference input is driven with a signal whose phase is jittered by a 40 ns p-p sine-wave at frequencies from 62.5 Hz to 8 kHz in octave steps. The p-p jitter at the output is measured at each step. AES-17 specifies that the jitter signal “is varied from 80 Hz to 20 kHz in octave steps.” Incrementing by octaves starting at 80 Hz does not get to 20 kHz. For simplicity sake, the jitter frequencies used here were chosen to be the same as the range used for jitter susceptibility measurements.

Sync Input Lock Range

Sync input lock range pertains to the risk that a converter will fail to lock to an external reference when there is a large difference between the external clock’s sample rate and the converter's internal clock’s sample rate. Large differences can cause problems with the converter achieving lock. There is an inherent tradeoff between a converters ability to lock to a wide deviation in reference frequency and its performance once locked.

The reference input is driven with a variable sample rate digital signal. The rate is varied from 48 kHz and the range over which the converter will lock is recorded. The reference should remain stable at each new frequency tested for at least 5 seconds before verifying lock.

Converters used to be expected to lock over a very wide range, typically up to 10% variation in sample rate. This stems from the desire to replace the “varispeed” function of analog tape recorders. This function is now implemented in digital processing devices and is no longer considered to be a requirement to address during signal capture. In this case a converter does not have to lock over as wide a range. Given the tradeoff on rejection of sync input jitter it is prudent to seriously consider the lock range required.

Device Field Testing and Specification Refinement

Background and General Conditions

This section compares measurements across the five devices tested. Objective performance measures produced quite different results on the five converters tested. The key results have been collected into tables to ease comparisons between converters.

Where IASA TC-04 limits exist they are included in the comparison tables. When a converter failed the performance limit the data is shown in red.

All measurements except Jitter Transfer Gain and Sync Input Lock Range were performed on all input channels. Significant differences are reported.

The measurements were performed at nominal line voltage +5% and -10% and any discrepancies are reported.

Each device under test was powered and operational for at least 30 minutes before measurements were performed.

The test equipment included devices from Qualis Test Systems, Audio Precision, Fluke and Tektronix, controlled by personal computer. In general, measurements were substantially above the test system residuals except when measuring the jitter and sideband performance for one of the ADCs.

The ambient temperature was maintained between 70 and 74 degrees Fahrenheit for all tests. The line voltage was controlled with a General Radio Variac (variable autotransformer) to allow spot testing at voltage extremes and to ensure consistent line voltage for the entire suite of measurements.

Frequency Response

All the converters tested passed the IASA TC-04 specification limits at 48 kHz except the defective channel on device 3[11], although that device and one other were very near the IASA "fail" point. One of these two also did not pass the 20 kHz response limit at the 96 kHz sample rate.

48 kHz Sample Rate

Frequency	IASA Limit	Device 1		Device 2		Device 3		Device 4		Device 5	
		Left	Right	Left	Right	Left	Right	Left	Right	Left	Right
20 - 20k Hz	+/- 0.1 dB	-0.03	+0.01	-0.03	+0.01	-0.10	-0.75	0.0	0.0	-0.09	-0.09

[11] Note, that this test and others revealed a failure in device 3 that was not evident otherwise, demonstrating the need to perform such tests.

96kHz Sample Rate

Frequency	IASA Limit	Device 1		Device 2		Device 3		Device 4		Device 5	
		Left	Right	Left	Right	Left	Right	Left	Right	Left	Right
20 – 20k Hz	+/- 0.1 dB	-0.02	+0.00	-0.02	+0.00	-0.10	-0.75	0.0	0.0	-0.13	-0.13
20k – 40k Hz	+/- 0.3 dB	-0.02	+0.05	-0.02	+0.05	-0.40	-0.75	+0.01	+0.01	-0.19	-0.19

Based on our findings we recommend the following performance specifications:

Sample Rate	Frequency	Limit
48kHz	20 – 20k Hz	+/- 0.1 dB
96kHz	20 – 20k Hz	+/- 0.1 dB
96kHz	20k - 40k Hz	+/- 0.5 dB

The amplitude tolerance change from +/-0.3 dB to +/-0.5 dB for the range 20kHz to 40kHz accommodates antialias filters with lower echoes and gentler phase behavior. It accommodates designs that use wide transition bands (for instance between 30kHz and 40kHz) to reduce the time-domain effects of a sharp filter, without practical negative implications.

THD+N

Components inside the converter often approach their operating limits as signals reach the device's maximum input level. Consequently distortion tends to dominate performance at levels very close to full scale. When handling high frequency signals these components may have difficulty keeping up with the high rate of change of the signal. This can cause distortion to rise at higher frequencies. Similarly, inadequately stiff power supplies or thermal effects can cause the converter to have issues handling very slowly changing signals. This manifests itself as increased low frequency distortion. The result is that the -1 dBFS distortion measurements at the three frequencies tested give a good picture of these issues. Note the performance of Device 2 and Device 4 at the higher amplitude in the table below.

48kHz Sample Rate Unweighted

Freq	Level	IASA Limit	Device 1		Device 2		Device 3		Device 4		Device 5	
Hz	dBFS		Left	Right	Left	Right	Left	Right	Left	Right	Left	Right
41	-1		-102.4	-106.3	-104.4	-104.3	-104.7	-102.6	-107.5	-106.9	-94.2	-94.7
997	-1	-105	-102.7	-106.0	-105.3	-105.5	-105.3	-105.6	-111.2	-110.5	-95.2	-96.4
6597	-1		-101.8	-104.7	-101.3	-100.7	-106.6	-106.3	-105.1	-105.4	-92.6	-93.3
41	-10		-99.5	-99.9	-99.9	-99.9	-106.3	-106.1	-103.5	-101.9	-95.9	-96.0
997	-10		-99.7	-100.1	-99.9	-99.9	-106.6	-106.3	-103.9	-102.7	-95.8	-96.2
6597	-10		-100.4	-100.7	-100.6	-100.1	-106.5	-106.2	-104.0	-102.6	-95.6	-96.0
41	-20		-91.4	-91.5	-91.0	-90.8	-98.0	-97.5	-94.8	-93.6	-89.2	-89.7
997	-20	-95	-91.6	-91.2	-91.0	-90.8	-98.1	-97.8	-95.3	-93.8	-89.6	-89.8
6597	-20		-91.6	-91.6	-91.7	-91.4	-98.4	-98.5	-95.7	-93.4	-90.1	-90.3
41	-60		-49.5	-49.8	-49.9	-49.6	-56.9	-56.4	-54.1	-52.7	-49.0	-49.3
997	-60		-50.8	-50.5	-49.9	-50.1	-57.2	-57.2	-54.2	-53.4	-49.3	-49.3
6597	-60		-51.1	-51.3	-50.4	-50.5	-57.5	-57.1	-54.4	-52.6	-46.2	-46.3

96kHz Sample Rate Unweighted

Freq	Level	IASA Limit	Device 1		Device 2		Device 3		Device 4		Device 5	
Hz	dBFS		Left	Right	Left	Right	Left	Right	Left	Right	Left	Right
41	-1		-101.9	-102.9	-104.4	-104.3	-104.6	-102.5	-107.4	-107.0	-93.4	-93.7
997	-1	-105	-101.5	-102.6	-105.3	-105.5	-105.5	-105.9	-110.6	-110.3	-94.5	-95.3
6597	-1		-97.8	-97.3	-101.3	-100.7	-106.8	-106.5	-105.0	-105.3	-92.1	-92.8
41	-10		-98.5	-99.0	-99.9	-99.9	-106.3	-106.1	-103.8	-103.1	-94.7	-95.0
997	-10		-98.1	-99.0	-99.9	-99.9	-106.5	-106.6	-103.7	-103.0	-94.9	-95.3
6597	-10		-98.5	-98.2	-100.6	-100.1	-106.4	-106.7	-103.9	-102.9	-94.9	-95.1
41	-20		-90.6	-90.5	-95.0	-94.1	-97.9	-97.1	-94.9	-94.1	-88.7	-88.7
997	-20	-95	-90.2	-90.5	-95.0	-94.2	-97.9	-97.4	-95.0	-94.2	-88.9	-89.2
6597	-20		-90.6	-90.2	-95.3	-94.4	-98.4	-98.3	-95.3	-94.4	-89.3	-89.7
41	-60		-47.7	-47.6	-49.9	-49.6	-56.9	-56.7	-54.1	-53.0	-49.0	-49.3
997	-60	-50	-49.9	-49.6	-49.9	-50.1	-56.8	-56.8	-54.1	-53.3	-49.2	-49.2
6597	-60		-50.0	-50.0	-50.4	-50.5	-57.7	-57.4	-54.7	-53.4	-49.7	-50.1

The frequency and level combinations highlighted in grey could be removed from the performance tests with no loss of completeness. Their presence serves mainly to observe the more important differences at the higher input levels.

Based on our findings we recommend the following performance specification:

Freq	Level	Limit (unweighted)
Hz	dBFS	
41	-1	-100
997	-1	-100
6597	-1	-100
997	-10	-100
997	-20	-90
997	-60	-50

Additional tests at lower amplitudes will demonstrate the way noise and distortion trade-off with each other. These rarely show frequency dependence as the noise begins to dominate the overall results. Whereas the IASA TC-04 specification provides reference points at -1dBFS and -20dBFS, we recommend two additional reference points be placed at -10dBFS, using a limit of -100dB unweighted, and -60dBFS, using a limit of -50dB. In addition to this, we recommend that performance specification limits be set for 41Hz and 6597 Hz in addition to 997Hz at the -1 dBFS amplitude. Implicit in this is the addition of these reference signals to the test method, following the same protocol as specified with the 997Hz signal. Based on our findings, we believe that these added data points will provide a more accurate reporting on the relevant THD+N characteristics of a given ADC.

Dynamic Range (Signal to Noise)

All converters except Device 3 failed the IASA TC04 limits.

	IASA Limit	Device 1		Device 2		Device 3		Device 4		Device 5	
		Left	Right	Left	Right	Left	Right	Left	Right	Left	Right
Unweighted	-115 dB	110.8	110.5	109.9	110.1	117.2	117.2	114.2	113.4	105.7	105.7
A weighted	-117 dB	113.1	113.4	112.4	112.3	119.4	119.7	116.7	116.3	108.6	108.6

Based on our findings we recommend the following performance specifications:

	Limit
Unweighted	-110 dB
A weighted	-112 dB

The failure of four of the five units suggested strongly that the IASA specification was too stringent. Relaxing the specification to the suggested values alleviates this issue while maintaining a level of stringency that we believe is appropriate for the intended application.

Cross-Talk

There is no IASA specification for cross-talk. We added cross-talk as a proposed performance specification with its own test method because of its strong implications to maintaining the integrity of the original recording. The performance specification required for cross-talk is highly dependent on the application. We believe that the varied applications in a preservation context mean that it is appropriate to use this somewhat demanding specification.

Frequency	Device 1		Device 2		Device 3*		Device 4		Device 5	
20 Hz	-131.3	-128.3	-162.2	-146.6			-129.9	-125.1	-103.9	-102.3
1k Hz	-111.7	-110.7	-133.6	-134.8			-137.4	-132.3	-109.3	-107.0
20 k Hz	-106.8	-110.7	-118.9	-116.1			-117.0	-120.0	-93.0	-92.3

Note: Results for Device 3 were unintentionally omitted.

The results demonstrate a great degree of variation in the performance of different converters, confirming the value of this performance parameter. Based on our findings we recommend the following specification:

Frequency	Limit
20 Hz	-120 dB
1k Hz	-120 dB
20 k Hz	-110 dB

We believe that the chosen limits are reasonable points of delineation separating the poorer-performing from the better-performing devices while maintaining an appropriate level of stringency. The proposed amplitude curve across the frequency range places frequencies that are predominant in the range of human hearing 10 dB beneath the noise floor. This limit is more stringent than the dynamic range limit based since dynamic range is based on a wideband performance measure while cross-talk is based on sinewave leakage from one channel to another.

A typical human observer is able to detect a tone and other information-carrying signals (e.g. speech, music) even at levels below the noise floor.

CMRR

There is no IASA specification for CMRR. It has been added as a proposed performance specification based on the fact that it indicates the ability of a device to reject noise that is not part of the incoming source signal, and the implications of this in the context of preservation. Higher dB values indicate better noise rejection.

Frequency	Device 1		Device 2		Device 3		Device 4		Device 5	
20 Hz	63.6	62.7	49.6	50.0	74.5	5.8	92.5	98.2	46.4	50.7
1k Hz	63.4	62.6	49.5	49.9	74.3	36.8	92.0	95.8	46.1	50.8
20 k Hz	56.8	54.0	49.4	49.8	75.9	55.4	68.9	72.8	46.1	50.8

Based on our findings, we recommend the following performance specification:

Frequency	Limit
60 Hz	70 dB
1k Hz	70 dB
20 k Hz	50 dB

Common mode interference is often due to power line issues making performance at low frequencies at least as important as mid band performance. Although the test was performed using a 20Hz it was decided to shift this to 60Hz.

The limits that have been set are based on analysis of the results and have been chosen to provide a specification that is simultaneously stringent and reasonable.

Intermodulation Distortion (IMD)

As mentioned previously, testing of both low frequency and high frequency intermodulation distortion occurred. Typically only the "sum" value is reported in performance specifications. Here we have reported the individual values in addition to the sum. In the case of the LF IMD test we have reported an additional metric labeled "integrated". This is an addition to the test method discussed earlier in this report, and provides the results using a classic SMPTE IMD analyzer.

LF IMD

All of the tested units would pass the proposed specification if it is implemented using spectrum analysis. If an analyzer that integrates sideband noise and distortion across the 40 Hz to 500 Hz range (a classic SMPTE IMD analyzer) were used, then one of the devices would fail. The rows highlighted in grey are primarily for informational purposes.

	IASA Limit	Device 1		Device 2		Device 3		Device 4		Device 5	
2nd		-103.0	-116.1	-119.4	-111.3	-112.9	-116.7	-110.4	-110.2	-93.9	-97.1
3rd	-	-108.7	-113.4	-99.2	-99.1	-101.8	-101.1	-107.1	-107.3	-99.3	-97.7
sum	-90 dB	-102.0	-111.5	-99.2	-98.8	-101.5	-101.0	-105.4	-105.5	-92.8	-94.4
integrated		-95.1	-102.1	-94.8	-94.3	-94.9	-95.4	-102.9	-102.6	-88.3	-90.5

HF IMD

All of the tested units pass the proposed limit, although one is close.

	IASA Limit	Device 1		Device 2		Device 3		Device 4		Device 5	
2nd		-105.7	-129.0	-137.9	-117.3	-115.8	<-140	<-140	<-140	-94.3	-97.5
3rd		-113.3	-112.4	-106.3	-105.5	-112.1	-111.9	-105.2	-105.5	-93.3	-93.2
sum	-90 dB	-105.0	-112.3	-106.3	-105.2	-110.6	-111.9	-105.2	-105.5	-90.8	-91.8

Based on our findings we recommend performing both Low Frequency and High Frequency tests, and reporting associated performance specifications:

Frequency	Limit
LF sum	-100 dB
HF sum	-105 dB

We propose tightening the IASA specification based on analysis of the results in order to provide a specification that is simultaneously stringent and reasonable. Furthermore, we recommend explicitly reporting of this specification as the ***sum*** measurement, since we have seen that manufacturers vary in their reporting of ***sum*** and ***integrated*** IMD measurements.

Amplitude Linearity

There are challenges in condensing the graphical results of this measurement down to single a numeric metric that may be compared to limits. The original IASA range from -115 dBFS to -5 dBFS is too wide and encounters large deviations near the noise floor which do not represent true amplitude linearity issues. Therefore we recommend changing this range to -105 dBFS to -5 dBFS. The peak deviation specification in the IASA document also provides some challenges in fairly representing converter differences. A single errant point can set the maximum positive or negative deviation without regard for how well behaved the remainder of the curve may be. Therefore we recommend using a standard deviation specification across the range of interest. This is included in the table below. All deviations noted are the largest positive or negative change from one point to another on the same curve.

	IASA Limit	Device 1		Device 2		Device 3		Device 4		Device 5	
Max + dev. -105 to -5	+0.5 dB	+0.05	+0.05	+0.12	+0.09	+0.02	+0.2	+0.12	+0.8	+0.1	+0.16
Max – dev. -105 to -5	-0.5 dB	-0.22	-0.10	-0.13	-0.08	-0.3	-0.2	-0.6	-0.6	-0.27	-0.07
Std. Dev.-105 to -5		0.008	0.038	0.114	0.096	0.020	0.182	0.023	0.035	0.046	0.019

Based on our findings and the discussion above we recommend the following specifications:

	Limit
Standard Deviation	0.05 dB

As discussed above, a change to analyzing and reporting standard deviation is recommended. The limit was selected based on analysis of the results and selecting a reasonable point of delineation.

Spurious Aharmonic Signals

	IASA Limit	Device 1		Device 2		Device 3		Device 4		Device 5	
60/180/300 Hz	< -130	-100.1	-100.1	<-100	<-100	-129.7	-129.7	<-103	<-103	<-130	<-130
120/240 Hz	< -130	-118.2	-118.2	<-100	<-100	-123.2	-123.2	<-103	<-103	<-129	<-129

Based on our findings we recommend loosening the IASA specification as follows:

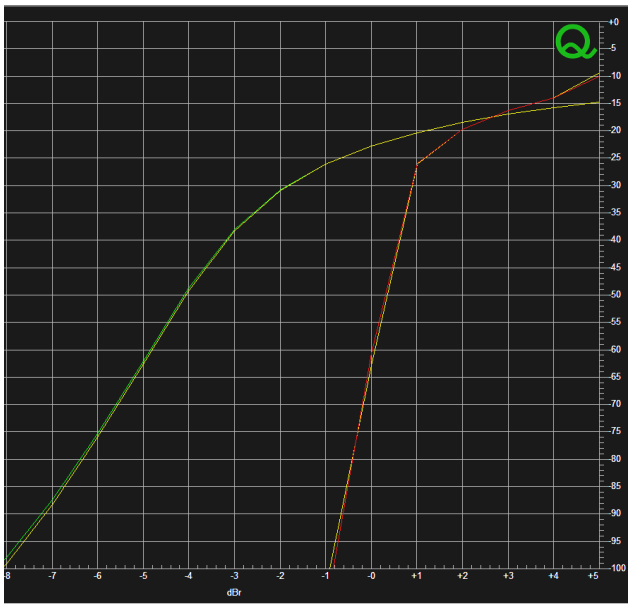
Frequency	Limit
> 50Hz	-100

The limit was set based on the results and establishing a more realistic specification.

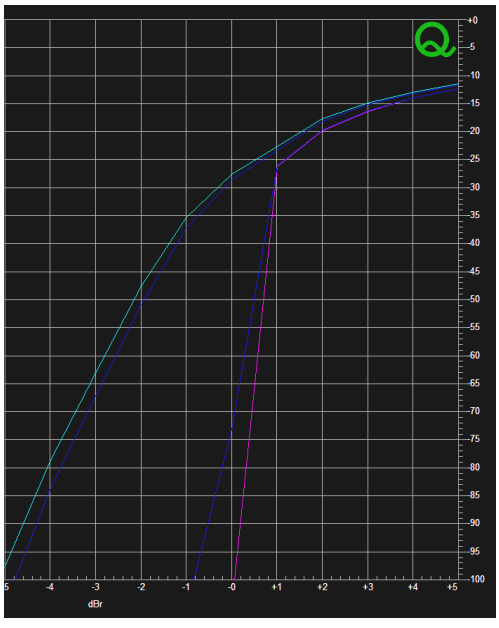
Input Overload Behavior

A proper numeric method of comparing overload behavior is still under development by AES committee SC-02-01. The converters tested all exhibited reasonable behavior when driven into overload. The measurement graphs are reproduced below.

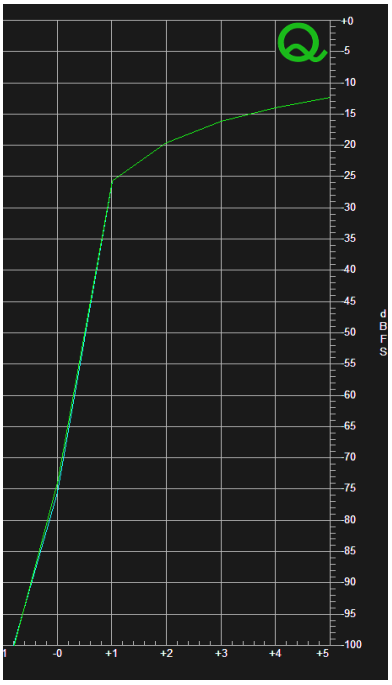
Device 1



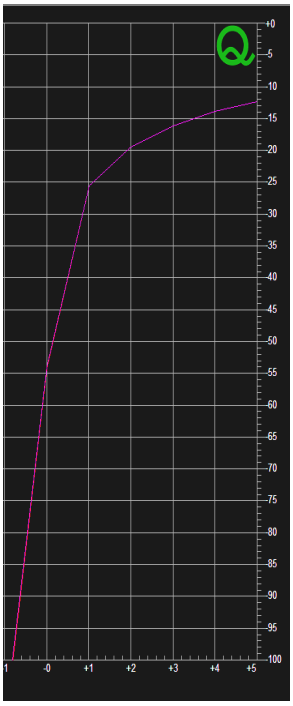
Device 2



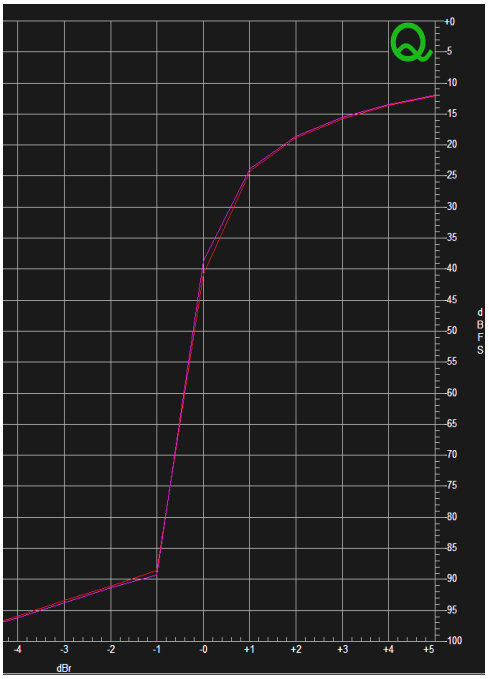
Device 3



Device 4



Device 5



Two of the professional units offer a special clipping management (limiter) functionality that can be turned off; we made two input overload measurements for each of these units, with the function turned off and turned on. Where the graphs above show two sets of curves (Device 1 & 2), one was made with the limiter function engaged and one with it off. The gradual rise, smooth curve, trace is with the limiter engaged. The result is gradually increasing distortion as signals approach full scale instead of an abrupt rise as full scale is reached. Due to time limitations, the effect on other measurements was not examined, but it is anticipated that it would result in significant differences in distortion and linearity performance.

There is no recommendation at this time for inclusion of this test method or a performance specification.

Alias Suppression

There is no specification for alias suppression in IASA TC-04. The results below identify the lowest frequency at which the alias component was equal to or greater in amplitude than all other alias components across the frequency range tested. Amplitude is expressed relative to the stimulus amplitude in dB.

SR	Device 1		Device 2		Device 3		Device 4		Device 5	
48 kHz	24 kHz	-96	27.5 kHz	-73	26.0 kHz	-98	27.7 kHz	-82	26.5 kHz	-88
96 kHz	24 kHz	-93	63 kHz	-72	51.9 kHz	-98	63.8 kHz	-80	53 kHz	-89

Based on our findings we recommend the following specifications:

SR	Limit
48 kHz	-80 dB
96 kHz	-80 dB

The proposed limits are based on analysis of the results and a determination of what represented a stringent yet reasonable specification.

Sync Input Jitter Susceptibility

There is no IASA performance specification for this parameter. Based on the implications for the common scenario of a converter referencing external synchronization, we believe that this metric is important. The jitter susceptibility of device 3 was extremely low, very near the limits of the measurement system. Not only was it highly resistant to jitter on its reference input but it introduced very little sideband noise on the test signal. Results are expressed as dBFS for each octave step.

12 kHz

Frequency	Device 1	Device 2	Device 3	Device 4	Device 5
8 kHz	-120.4	-129.4	-142.7	-141.1	-117.1
4 kHz	-108.4	-115.4	-138.2	-135.9	-50.3
2 kHz	-94.1	-101.7	-137.7	-133.7	-44.0
1 kHz	-79.6	-86.3	-122.5	-122.9	-99.3
500 Hz	-63.5	-75.3	-125.4	-108.7	-93.3
250 Hz	-55.4	-69.6	-117.5	-90.7	-87.4
125 Hz	-56.7	-63.3	-118.3	-70.5	-81.1
63 Hz	-56.3	-59.6	-118.3	-63.2	-75.0

997 Hz

Frequency	Device 1	Device 2	Device 3	Device 4	Device 5
500 Hz	-100.2	-96.6	-138.2	-129.2	-114.3
250 Hz	-76.2	-87.0	-139.5	-111.6	-108.4
125 Hz	-77.3	-80.0	-132.5	-92.2	-102.5
63 Hz	-77.9	-76.3	-122.1	-84.8	-96.7

Based on our findings, we recommend the following specifications:

12 kHz

Frequency	Limit
8 kHz	-130 dB
4 kHz	-120 dB
2 kHz	-120 dB
1 kHz	-120 dB
500 Hz	-100 dB
250 Hz	-90 dB
125 Hz	-70 dB
63 Hz	-60 dB

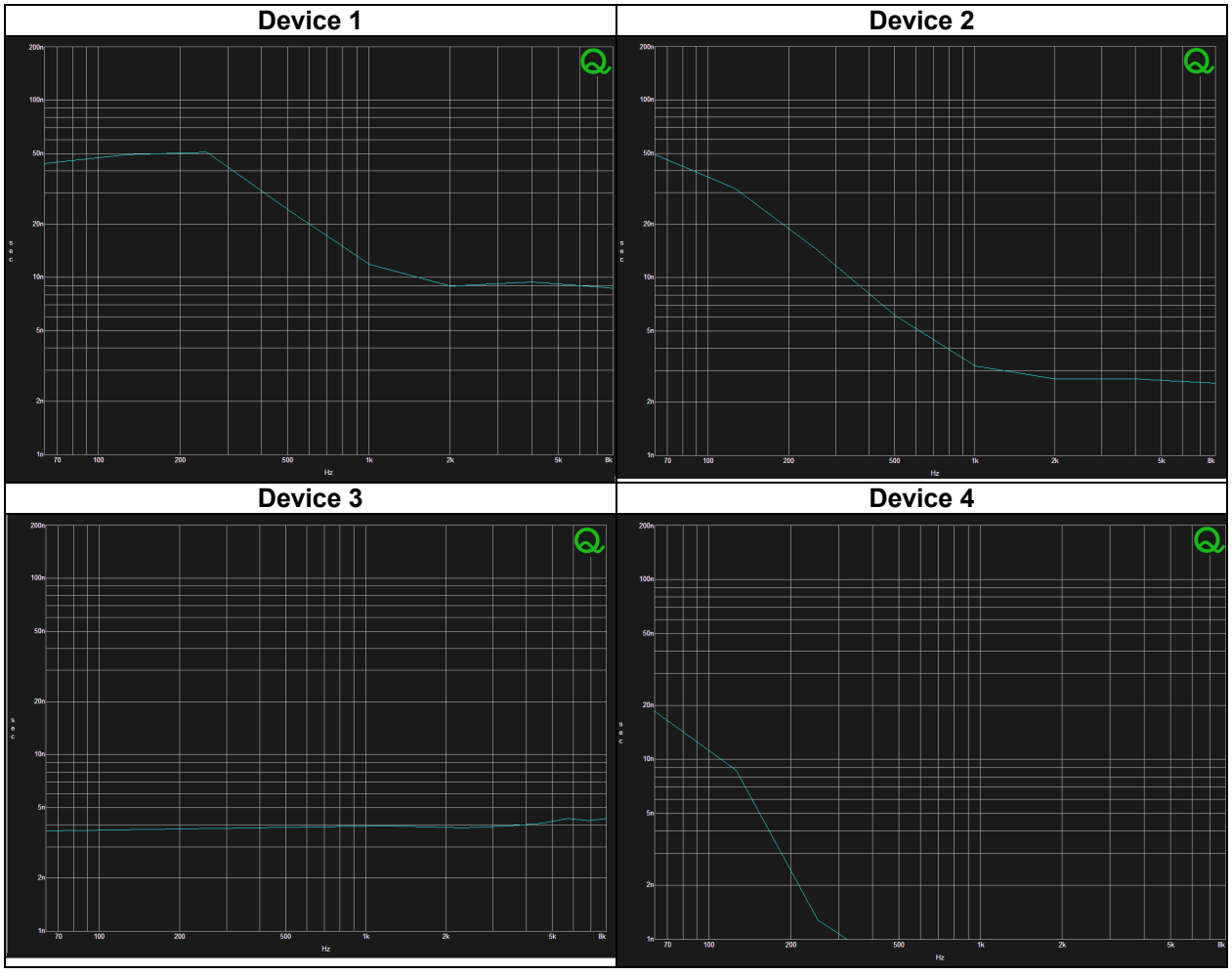
997 Hz

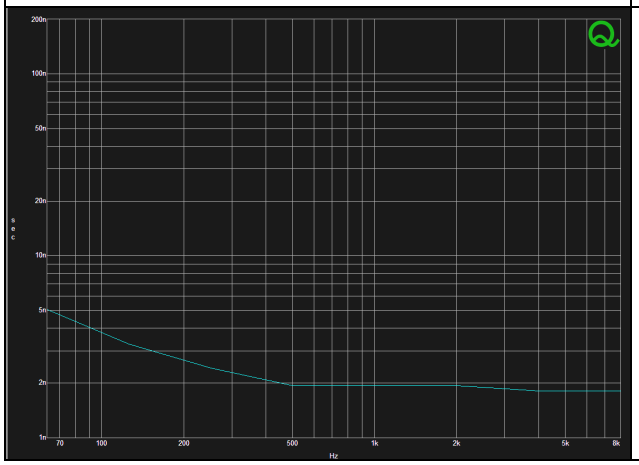
Frequency	Limit
500 Hz	-110 dB
250 Hz	-100 dB
125 Hz	-90 dB
63 Hz	-80 dB

The referenced frequencies are implicit in the test method. The limits are based on analysis of the results and a determination of what was both stringent and reasonable.

Jitter Transfer Gain

This specification is a variation on IASA's *Jitter* performance specification. This test assesses *jitter gain* as a result of jitter referenced against the jitter at the sync input. The addition of this reference point provides a meaningful look into the implications to the audio signal. Measuring interface jitter alone does not give an indication of the impact to audio performance. Interface jitter and sampling jitter are two distinct metrics and measuring the former does not provide a direct link to assessing the latter.



Device 5	
	

Based on our findings we recommend the following specifications:

Limit
< 20ns p-p

The limit was chosen based on assessing the range found within the results and making a determination of what was simultaneously stringent yet reasonable.

Sync Input Lock Range

	IASA Limit	Device 1		Device 2		Device 3		Device 4		Device 5	
Lock	2%	<-1%	>+1%	<-1%	>+1%	-0.016%	+0.014%	<-1%	>+1%	<-1%	>+1%
Acquire	2%	<-1%	>+1%	<-1%	>+1%	-0.012%	+0.009%	<-1%	>+1%	<-1%	>+1%

The tradeoff between jitter rejection and Sync Input Lock Range showed dramatically. However, monitoring THD+N and Spurious Aharmonic Signals demonstrated that all units performed as well when operating at the limits of their lock range as they did when locked to a nominally correct signal. In addition to this, 2% tolerance is much wider than necessary and represents locking to a grossly inaccurate reference. There is very little practical application that justifies such a wide tolerance. Furthermore, there is a direct tradeoff with jitter rejection as evidenced by the excellent rejection performance of device #3 compared to all the other units. The lack of practical application and the implicit worsening of jitter rejection does not justify specifying a wider lock range. Based on our findings, we recommend omitting this test method and performance specification.

Field Test Summary and Conclusions

The preceding summary of the findings of our field test clearly supports the need for the performance testing of ADCs. As noted earlier, in terms of testing ADC devices, this field test was not statistically valid; the test was not run on multiple instances of a given ADC. Nevertheless, it is worth noting that in this group of five, two were very good performers, two

were in the middle, and one was noticeably worse. The devices tend to excel and fall short on different performance facets, no doubt revealing the design tradeoffs that face all manufacturers.

The findings of this field test, as well those developed during the analysis that preceded it, as summarized in part I of this document, have led the FADGI Audio-Visual Working Group to recommend some adjustments to the IASA Performance Specifications and the associated test methods. The final approved recommendation is provided in the August 2012 *Guideline for Audio Analog-to-Digital Converter Performance Specification and Test Method.*[12]

As part of this process, there was a public comment period from February to July 2012 during which feedback was requested and received.[13] In some cases, these comments informed the edits in this finalized version of the report and the changes made will obscure the original references. In other cases, the comments received will inform next steps and future work. A debt of gratitude is owed to those who took the time to review and provide valuable feedback on this report and the associated guideline.

[12] http://www.digitizationguidelines.gov/audio-visual/documents/A2D_performGuide_2012005xx.pdf
[13] A summary of the comments is provided at http://www.digitizationguidelines.gov/audio-visual/documents/Comment_summary_20120712.pdf and http://www.digitizationguidelines.gov/audio-visual/documents/Comment_summary_20120621.pdf.

Appendix: Comparison to IASA TC-04

IASA's TC 04[14] serves as a critical benchmark and starting point for the FADGI guideline. It is a familiar source to virtually every worker in the field of audio preservation. The FADGI guideline recommends some adjustments to the TC-04 metrics but the importance of the IASA document is acknowledged by this appendix, offering a side-by-side presentation of both sets of recommendations in order to facilitate comparison.

<table>
<tr><td>Test Name</td><td colspan="3">Frequency Response</td></tr>
<tr><td>Test Method</td><td colspan="3">According to AES-17: Frequency response shall be measured at –20 dBFS with a sinewave whose frequency varies from 10 Hz to 50 kHz in steps no larger than 10 per octave.</td></tr>
<tr><td>Performance Specification</td><td colspan="3"><table>
<tr><th>Sample Rate</th><th>Frequency</th><th>Limit</th></tr>
<tr><td>48kHz</td><td>20 – 20k Hz</td><td>+/- 0.1 dB</td></tr>
<tr><td>96kHz</td><td>20 – 20k Hz</td><td>+/- 0.1 dB</td></tr>
<tr><td>96kHz</td><td>20k - 40k Hz</td><td>+/- 0.5 dB</td></tr>
</table></td></tr>
<tr><td>IASA Specification</td><td colspan="3">Frequency Response: For an A/D sampling frequency of 48 kHz, the measured frequency response will be better than ± 0.1 dB for the range 20 Hz to 20 kHz. For an A/D sampling frequency of 96 kHz, the measured frequency response will be better than ± 0.1 dB for the range 20Hz to 20 kHz, and ± 0.3 dB for the range 20 kHz to 40 kHz. For an A/D sampling frequency of 192 kHz, the frequency response will be better than ± 0.1 dB for the range 20Hz to 20 kHz, and ± 0.3 dB from 20 kHz to 50 kHz (reference audio signal = 997 Hz, amplitude -20 dB FS).</td></tr>
</table>

<table>
<tr><td>Test Name</td><td colspan="3">Total Harmonic Distortion + Noise (THD+N)</td></tr>
<tr><td>Test Method</td><td colspan="3">Based on AES-17: The EUT shall be stimulated with a low distortion sine wave. The test signal present in the output shall be removed with a notch filter and bandwidth limited from 20 Hz to 20 kHz. The RMS amplitude is reported as a ratio to the RMS amplitude of the unfiltered signal. The measurement should be performed at the following amplitude and frequency combinations: -1.0 dBFS at 41 Hz, 997 Hz and 6597 Hz, –10 dBFS at 997 Hz, and -20 dBFS at 997 Hz, and -60 dBFS at 997 Hz.</td></tr>
<tr><td>Performance Specification</td><td colspan="3"><table>
<tr><th>Freq</th><th>Level</th><th>Limit (unweighted)</th></tr>
<tr><td>Hz</td><td>dBFS</td><td></td></tr>
<tr><td>41</td><td>-1</td><td>-100</td></tr>
<tr><td>997</td><td>-1</td><td>-100</td></tr>
<tr><td>6597</td><td>-1</td><td>-100</td></tr>
<tr><td>997</td><td>-10</td><td>-100</td></tr>
<tr><td>997</td><td>-20</td><td>-90</td></tr>
<tr><td>997</td><td>-60</td><td>-50</td></tr>
</table></td></tr>
</table>

[14] International Association of Sound and Audiovisual Archives (IASA) Technical Committee. *TC 04: Guidelines on the Production and Preservation of Digital Audio Objects*, ed. by Kevin Bradley. Second edition 2009. Available from www.iasa-web.org/tc04/audio-preservation.

IASA Specification	Total Harmonic Distortion + Noise (THD+N): With signal 997 Hz at -1 dB FS, the A/D converter THD+N will be less than -105 dB unweighted, -107 dB A-weighted, 20 Hz to 20 kHz bandwidth limited. With signal 997 Hz at -20 dB FS, the A/D converter THD+N will be less than -95 dB unweighted, -97 dB A-weighted, 20 Hz to 20 kHz bandwidth limited.

Test Name	**Dynamic Range (Signal to Noise)**
Test Method	Based on AES-17: The measurement is the ratio of the full-scale amplitude to the weighted r.m.s. noise and distortion, expressed in dB, in the presence of signal. It includes all harmonic, inharmonic, and noise components. The test signal shall be a 997-Hz sine wave producing – 60 dBFS at the EUT output. Any 997-Hz test signal present in the output is removed by means of a standard notch filter. The remaining noise is filtered with an A weighting filter limited to 20 kHz. The results shall be reported as unweighted and A-weighted in dBFS.
Performance Specification	**Weighting** / **Limit** Unweighted / -110 dB A weighted / -112 dB
IASA Specification	Dynamic Range (Signal to Noise): The A/D converter will have a dynamic range of not less than 115 dB unweighted, 117 dB A-weighted. (Measured as THD+N relative to 0 dB FS, bandwidth limited 20 Hz to 20 kHz, stimulus signal 997 Hz at -60 dB FS).

Test Name	**Cross-Talk**
Test Method	One channel of the EUT is driven with a -1 dBFS sinewave and the maximum amplitude of this frequency appearing in any other channel is noted. The measurement is repeated for each input channel and the maximum amplitude for all channels is determined. This amplitude, expressed in dBFS, is increased by 1 dB and reported. The measurement shall be performed at frequencies of 20 Hz, 1 kHz and 20 kHz.
Performance Specification	**Frequency** / **Limit** 20 Hz / -110 dB 1k Hz / -110 dB 20 k Hz / -105 dB
IASA Specification	No equivalent specification

Test Name	**Common-Mode Rejection Ratio (CMRR)**
Test Method	The input shall be driven from a sinewave generator whose output impedance is less than 100 Ohms. The amplitude is adjusted to achieve -20 dBFS at the EUT output. The signal is removed, and the generator reconnected between the chassis ground and one side of the input. A 600 Ohm resistor is connected between this point and the other side of the input. If the input is asymmetrical, the generator should be connected to the low side and the resistor to the high side. The output should be measured through a bandpass filter at the

	sinewave frequency. The resulting RMS value, measured in dBFS, is increased by 20 dB and reported as a dB (not dBFS) value. The measurement should be performed at 60 Hz, 1 kHz and 20 kHz.
Performance Specification	**Frequency** / **Limit** 60 Hz / 70 dB 1k Hz / 70 dB 20 k Hz / 50 dB
IASA Specification	No equivalent specification

Test Name	**Low Frequency Intermodulation Distortion (LF IMD)**
Test Method	Based on AES-17: IM measurements shall be performed with a twin tone signal with a peak amplitude of -1.0 dBFS. The lrms sum of second- and third-order difference frequency components in the output are measured and reported in dBFS. The test frequencies shall be 41 Hz and 7993 Hz in a 4:1 amplitude ratio.
Performance Specification	**Frequency** / **Limit** LF sum / -100 dB
IASA Specification	Intermodulation Distortion (IMD): The A/D converter IMD will not exceed -90 dB. (AES17/SMPTE/DIN twin-tone test sequences, combined tones equivalent to a single sine wave at full scale amplitude).

Test Name	**High Frequency Intermodulation Distortion (HF IMD)**
Test Method	Based on AES-17: IM measurements shall be performed with a twin tone signal with a peak amplitude of -1.0 dBFS. The lrms sum of second- and third-order difference frequency components in the output are measured and reported in dBFS. The test frequencies shall be 20 kHz and 18 kHz in a 1:1 amplitude ratio.
Performance Specification	**Frequency** / **Limit** HF sum / -105 dB
IASA Specification	Intermodulation Distortion (IMD): The A/D converter IMD will not exceed -90 dB. (AES17/SMPTE/DIN twin-tone test sequences, combined tones equivalent to a single sine wave at full scale amplitude).

Test Name	**Amplitude Linearity**
Test Method	Based on AES-17: Level-dependent logarithmic gain is measured at 997 Hz from -5 dBFS to -105 dBFS and reported as standard deviation value in dB.
Performance Specification	**Limit** Standard Deviation / 0.05 dB
IASA Specification	Amplitude Linearity: The A/D converter will exhibit amplitude gain linearity of ± 0.5 dB within the range -120 dB FS to 0 dB FS. (997 Hz sinusoidal stimuli).

Test Name	**Spurious Aharmonic Signals**
Test Method	A 997 Hz sinewave shall be applied at -1 dBFS. The output spectrum shall be measued with an 32,768 point FFT. The largest inharmonic component is reported in dBFS.
Performance Specification	**Frequency** | **Limit** > 50Hz | -100
IASA Specification	Spurious Aharmonic Signals: Better than -130 dB FS with stimulus signal 997 Hz at -1 dBFS

Test Name	**Alias Rejection**
Test Method	Based on AES-17 and IEC 61606-3: The device is stimulated with a variable frequency sine wave at -10 dBFS. Beginning at half the sample rate, the frequency is continuously increased until it reaches 200 kHz. For a 48 kHz sample rate, the frequency is swept from 24 kHz to 200 kHz. For a 96 kHz sample rate, the frequency is swept from 48 kHz to 200 kHz. The rms amplitude at the converter output, increased by 10 dB, is graphed. Results are reported as the lowest frequency at which the alias component was equal to or greater in amplitude than all other alias components across the frequency range tested. Amplitude is expressed relative to the stimulus amplitude in dB.
Performance Specification	**SR** | **Limit** 48 kHz | -80 96 kHz | -80
IASA Specification	No equivalent specification

Test Name	**Sync Input Jitter Susceptibility**
Test Method	Based on AES-17: The converter input is driven with a -3 dBFS low distortion sinewave at 12 kHz. The reference input is driven with a signal whose phase is jittered with a 40 ns p-p sine-wave whose frequency varies from 62.5 Hz to 8 kHz in octave steps. The output spectrum is measured at each step and the results overlaid. The measurements are repeated with a 997 Hz input to the converter. Results are expressed as dBFS for each octave step.
Performance Specification	12 kHz **Frequency** | **Limit** 8 kHz | -130 dB 4 kHz | -120 dB 2 kHz | -120 dB 1 kHz | -120 dB 500 Hz | -100 dB 250 Hz | -90 dB 125 Hz | -70 dB 63 Hz | -60 dB 997 Hz **Frequency** | **Limit** 500 Hz | -110 dB 250 Hz | -100 dB 125 Hz | -90 dB 63 Hz | -80 dB
IASA Specification	No equivalent specification

Test Name	**Jitter Transfer Gain**
Test Method	Based on AES-17: The reference input shall be driven with a signal whose phase is jittered with a 40 ns p-p sine-wave jitter signal whose frequency varies from 62.5 Hz to 8 kHz in octave steps. The p-p jitter at the output shall be measured at each step and the results shall be graphed. Results shall also report the maximum p-p jitter value in ns.
Performance Specification	**Limit** < 20ns p-p
IASA Specification	Jitter (related but not equivalent): Interface jitter measured at A/D output <5ns (related but not equivalent)

Test Name	**Internal Sample Clock Accuracy (IASA)**
Performance Specification	No equivalent FADGI specification
IASA Specification	For an A/D converter synchronised to its internal sample clock, frequency accuracy of the clock measured at the digital stream output will be better than ±25 ppm

Test Name	**External Synchronization (IASA)**
Performance Specification	No equivalent FADGI specification
IASA Specification	Where the A/D converter sample clock will be synchronised to an external reference signal, the A/D converter must react transparently to incoming sample rate variations ± 0.2% of the nominal sample rate. The external synchronisation circuit must reject incoming jitter so that the synchronised sample rate clock is free from artefacts and disturbances.