Federal Agencies Audio Visual Digitization Working Group

Analog-to-Digital Converter Performance Specification and Testing

Study and Recommended Guideline

Prepared
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Background

This report was commissioned by the Federal Agencies Audio-Visual Working Group, part of the Federal Agencies Digital Guidelines Initiative (FADGI).[1] Chris Lacinak is the principle investigator and author. During the development and drafting of this report, Lacinak received valuable guidance from a number of individuals, notably Richard Cabot[2] and Ian Dennis.[3] Cabot provided support with creating the test suite, performing the tests, and providing expert feedback on the performance specifications. Dennis provided extensive feedback which greatly informed the creation of the test suite and associated performance specifications.

The Federal Agencies Audio-Visual Working Group wishes to develop a set of concepts, specifications, metrics, and measurement methods that pertain to the performance of the systems used to digitize sound recordings. (The scope for this activity does *not* include the intricacies of the playback of historical materials such as discs, tapes, and cylinder recordings.) System performance in the broadest sense includes the metrics discussed in this document and also the issues associated with *interstitial errors*, where samples are dropped or otherwise altered in the final digital audio file. Interstitial errors and their identification are the topics of a separate still-in-process report for the Working Group by Audiovisual Preservation Solutions.

This report focuses on the performance of the analog-to-digital converters (ADCs) used in reformatting workflows. Although other devices, cables, or interfaces in the signal chain can influence some of the performance aspects discussed here, this topic is beyond our scope at this time. The Working Group is interested in the reformatting of historical sound recordings and not in the creation of new recordings in the studio or in the field. It is the case, however, that many of the issues and metrics under discussion here are equally relevant for the creation of new recordings.

Three aspects of performance are explored in this document: (1) which parameters or features warrant measurement in the first place, (2) what performance specifications are appropriate for high quality content in an archival context and (3) what methods ought to be used to make the measurements? There are two critical starting points for answering these questions. First, an excellent listing of parameters and performance specifications are provided in *TC 04: Guidelines on the Production and Preservation of Digital Objects, 2nd ed., 2009*,[4] published by the International Association of Sound and Audiovisual Archives (IASA). Although this report recommends some adjustments to TC-04, it is still the case that the preservation community owes a great debt to this important work. Second, the best sources for methods are two documents that have emerged from the Audio Engineering Society (AES) Standards Working Group SC-02-01. These documents are *AES17-1998 (r2009): AES standard method for digital*

[1] http://www.digitizationguidelines.gov/
[2] Richard C. Cabot has a Ph.D. from Rensselaer Polytechnic Institute and his professional career has included work at Tektronix, Audio Precision (which he co-founded), XFRM, Inc., and Qualis Audio. Cabot also chairs the committee that developed the AES-17 digital audio measurement standard.
[3] Ian Dennis is the co-founder and Chief Technical Officer at Prism Sound, a well-known manufacturer of digital audio systems. .
[4] Web version and pdf download available at http://www.iasa-web.org/tc04/audio-preservation

audio engineering — Measurement of digital audio equipment (Revision of AES17-1991)[5] and *IEC-61606-3 Audio and audiovisual equipment - Digital audio parts - Basic measurement methods of audio characteristics - Part 3: Professional use.* The writer of this document is a member of the Audio Engineering Society standards committee SC-02-01which is involved in continued refinement of these standards. While AES-17 is used as the primary reference, both aforementioned standards and the ongoing work in support of their continued refinement informed the drafting of this document.

Recommended Guideline and Levels of Achievement

The previous version of this document was discussed at the December 8, 2011, meeting of the Working Group. The group's consensus was that the next iteration of the document--this one--should be posted on the FADGI Web site for public comment. Readers should note that the main part of this document is explanatory while appendix A provides the draft guideline for ADC performance metrics and measurement methods. The chair of the Working Group has informed this writer that this document is open for comment until April 15, 2012. Following this period, the comments will be reviewed and the recommendations will be revised as needed. Then the revised recommendations will be posted as an approved FADGI guideline.

General ideas about audio digitization system performance were outlined in the March 15, 2011, report titled *Assess Audio System Evaluation Tools: Initial Report*.[6] One important idea concerned levels of achievement. The March report notes the existence of many different archival organizations and the wide range of categories of material to be reformatted.

> Either or both of these variables may occasion variation in the quality of the preservation copies that are produced. In many archives, curators will indicate which classes of content warrant expert, high end treatment and which may be reformatted using moderate means. In addition, practical matters will influence production planning: limitations on budgets and human resources and the availability or unavailability of high quality studio workrooms. (p. 7)

Quality variation will generally be a matter of "curator's choice," with some reformatting projects seeking to produce the highest quality copies while others produce copies at moderate quality levels. Thus the most stringent specifications apply to the highest quality efforts with more relaxed specifications applied to moderate quality projects. In a parallel effort by the Federal Agencies Still Image Working Group, four performance levels have been associated with the same set of target specifications. All levels have the same "aim points," but they allow for varying tolerances, i.e., the highest performance level allows very little variation from the target value while the lowest performance level allows for a much greater level of variation.

The recommendations in appendix A are for the highest level of performance for analog-to-digital converters. The Working Group has not yet developed relaxed pass-fail levels but plans to in the near future. The group anticipates that, like the Still Image Working Group, these

[5] http://www.aes.org/publications/standards/search.cfm?docID=21
[6] http://www.digitizationguidelines.gov/audio-visual/documents/FADGI_Audio_EvalPerf_Report.pdf

relaxed levels will have the same aim points for various metrics but will permit wider deviation in the values achieved.

Introduction and Overview

The second edition of IASA TC-04 was published in 2009 and it presents the IASA technical committee's specifications for ADCs used for preservation purposes. In July 2011, the Federal Agencies Working Group commissioned AudioVisual Preservation Solutions to examine and report on the sufficiency and stringency of the IASA TC-04 performance specifications and the associated test methods (i.e., the documented tests performed to ascertain the resulting performance specification).

When the study was first raised in the Working Group, some members asked about the necessity for such testing. The discussion revolved around a pair of questions that have been followed as this report was drafted.

> **Is there a need to independently measure ADCs? Every ADC manufacturer publishes specifications which obviates the need to do additional testing.**
>
> For several years, audio professionals have argued that the performance specifications distributed by audio equipment manufacturers fail to provide complete statements of what has been measured or about the test methods employed. These specifications do not permit easy comparison of ADCs in the marketplace. This circumstance makes it difficult for an archive to compare ADCs when planning a purchase or, when outsourcing, to evaluate the equipment that a service bureau proposes to use.
>
> In the course of this study, we carried out two supporting activities were performed in order to generate additional data points in response to the question. First, published specifications were downloaded for several ADCs and compared against the IASA TC performance specifications. The aforementioned issues quickly became apparent. In some cases, there was no published specification to compare to the IASA TC performance specification. In other cases, the framing of the published specification made it challenging to compare to the IASA specification. Furthermore, in many cases the test method used to produce the specification was not reported, making it challenging to perform a comparison.
>
> In addition to this the question was posed to the Audio Engineering Society standards committee SC-02-01 (responsible for AES-17) for feedback. This committee includes representative of ADC manufacturers as well as independent test and measurement experts. Responses confirmed that the manufacturers' published specifications do not support meaningful comparative analysis.
>
> **Once an ADC is verified to perform properly does it need to be tested on an ongoing basis? A high quality ADC will not fail except for in very obvious ways, eliminating the need to perform routine testing.**

> Historically, standard operating procedure in professional audio studio environments includes testing the performance and integrity of equipment and signal paths on a regular and ongoing basis. Some specialists who provided comments as this study took shape, however, asserted that the dependability and failure modes of current high quality ADCs render costly routine testing and measurement unnecessary. This assertion was also presented to SC-02-01 for feedback. The committee members were unanimously in favor of routine testing, reached consensus that ADCs are no different than any other type of equipment, and stated that ADCs can fail in nuanced and subtle ways, on both analog input and digital output.

The discussions with experts and others in the audio community gave us confidence that having independent measurement and performance monitoring would indeed contribute to more reliable preservation transfers. Having confirmed the value of this investigation, our process began by identifying standardized test methods associated with each IASA performance specification. These largely referenced the Audio Engineering Society AES-17, *AES standard method for digital audio engineering – Measurement of digital audio equipment.*

Framing the analysis

The background statement above highlights three aspects of general concern in this document: *how* and *what* to measure, and what are *acceptable results*. It also identified two key documents: IASA TC-04 and AES-17. We restated these three elements in a more specific way in order to frame this analysis:

- Are the IASA performance specifications set at the appropriate level of stringency for a standard representing the highest level of required performance for preservation purposes?
- Are the number and types of tests being performed sufficient and appropriate to assess the quality of an ADC for preservation purposes?
- For any new test methods proposed for inclusion in the core test suite that do not have IASA performance specification counterparts, what is the recommended performance specification?

Feedback was sought on these questions from ADC manufacturers, test and measurement companies, and the Audio Engineering Society standards committee SC-02-01. Although the interest in maintaining a minimal approach was understood, consensus indicated that the proposed IASA/AES test suite would benefit from being more comprehensive in order to properly assess the quality of ADCs. The individuals we consulted recommended a number of additional tests and we used their collective feedback to create a test suite that expanded upon the original IASA performance specifications and associated test methods. Using the larger test suite would reveal both the sufficiency of the original test set, as well as the significance of additional test methods and performance specifications. It is worth noting that AES-17 is currently under revision. The revision points were taken into consideration for inclusion in this study as well.

Testing to refine the metrics

As the modified test suite and performance specifications were being drafted, a set of field tests were devised. These consisted of carrying out performance tests on five ADC devices, including examples of converters currently used by various Federal Agencies and covering a range of price

points and published technical specifications. We emphasize that this was not intended to be a test of these devices per se, but rather a way for us to assess the efficacy of the metrics and methods we were developing. It is also the case that only one instance of each device was tested, in contrast to a proper device test where multiple instances would be tested in order to reduce the risk of sample-specific defects. For all of this reasons, we do not identify the devices in this report.

The converters offered different combinations of output formats, input limiting circuitry, dithering processes and number of channels. Although four of the five units included digital-to-analog converters (DAC), this was not considered in scope for this study and was not evaluated. Two of the five units were multichannel devices and the other three were two-channel devices. Testing was limited to two channels of each device.[7] Where multiple choices of dither were available, the testing was limited to flat spectrum triangular dither. These simplifications were made for schedule reasons and to ensure units were compared under similar conditions.

Following testing, the results were analyzed relative to each other and to the originating performance specifications. Resulting findings and recommendations are discussed in detail below.

Test Suite

Many measurements in this suite follow the techniques specified in AES-17 and are cited as such. The procedures in AES-17 apply to analog-to-digital, digital-to-analog, and digital-to-digital devices. As this study is primarily focused on ADCs, in many cases the procedures may be simplified. Modifications to the referenced standards are noted where applicable.

A reference level of +18 dBu was chosen as the analog equivalent of digital full scale. This is a common reference level in modern studios and broadcast facilities. Initial measurements on the converters verified that this was usable for all units.[8] Each converter's gain was adjusted to make a +18 dBu input result in 0 dBFS out.

The descriptions that follow are included to facilitate understanding of the test results. They are written in descriptive style, rather than the requirements style used in standards, and are concise. The following test suite represents the tests performed as part of the study and is not the recommended final test suite. The final recommended test suite is provided in the summary and conclusions portion of this report.

Frequency response

Frequency response assesses the constancy of gain across frequency, demonstrating the converters' ability to capture the signal without "coloring" its sound. For converters this is generally a flat line across most of the audio band, deviating only at very low and very high frequencies.

[7] Except in one instance where we determined that the performance of the front panel and rear panel line level inputs differed significantly, warranting assessment and reporting of both.
[8] This was later discovered to be sub-optimal for the device as discussed below. Additional measurements were made on the device unit as a result.

The measurement is performed with a variable frequency sinewave input and an rms amplitude measurement at the output. The sinewave frequency is swept from 10 Hz to 50 kHz using 10 steps per octave. The sinewave amplitude is 20 dB below full scale to allow margin for non-flat converter response without clipping the output and to reduce the chance of nonlinear behavior at the frequency extremes.

This is the procedure specified in AES-17. The measurement is performed at both 48 kHz and 96 kHz sample rates.

Total Harmonic Distortion plus Noise (THD+N)

THD+N is a basic test of converter distortion and is used to assess the amount of "junk" added to a clean audio signal. Since the measurement depends on quantifying the harmonics added to a clean sinewave it is of limited utility at high frequencies where the limited bandwidth of the digital audio format may prevent the harmonics from appearing in the output.

The ADC is driven with a low distortion sine wave. The digital output is passed through a notch filter, bandwidth limited from 20 Hz to 20 kHz and the RMS amplitude measured. The THD+N is the ratio of this value to the RMS amplitude of the unfiltered signal. The measurement is performed at all combinations of the amplitudes -1.0 dBFS, -10 dBFS, -20 dBFS and -60 dBFS and frequencies of 41 Hz, 997 Hz and 6597 Hz. The upper frequency is chosen to allow both 2nd and 3rd harmonics to pass through a 20 kHz bandwidth limited digital interface.

This procedure follows the AES-17 standard, differing only in the frequency and level combinations employed. The measurement is performed at both 48 kHz and 96 kHz sample rates.

Dynamic Range/Signal to Noise Ratio

Dynamic range is an approximation to the perceived noise in the converter, giving an indication of the widest dynamic range which may be accommodated when using the converter.

The ADC is driven with a low amplitude, mid frequency sine wave (-60 dBFS, 997 Hz). This ensures that the converter is active rather than producing a static digital output value. The sinewave is removed from the output using a digital notch filter resulting in a signal representative of the noise generated by the converter. This is passed through a weighting filter (A-weighting, band limited to 20 kHz, for these measurements) to simulate the ears sensitivity at low levels. The rms amplitude is measured and expressed in dB relative to full scale (dBFS).

This differs from AES-17 in that A-weighting is used in place of CCIR weighting. Measurements are also made unweighted, with a 20 Hz to 20 kHz bandwidth limit. Both are reported for each channel, giving a total of 4 measurements.

Intermodulation Distortion

The AES-17 test method provides the option of performing a Low Frequency (LF) test and a High Frequency (HF) test for *Intermodulation Distortion (IMD).*

High Frequency Intermodulation Distortion

High frequency intermodulation distortion (HF IMD) is an alternative test of converter distortion. By using two closely spaced high frequency sinewaves and measuring the modulation they induce on each other it is possible to measure nonlinearities at frequencies close to the high frequency bandwidth limit of the converter.

The converter is driven with two equal amplitude high frequency sinewaves (18 kHz and 20 kHz) whose combined peak-peak amplitude reaches 1 dB below the full scale input amplitude. The full output spectrum is provided graphically. The sum of second- and third-order difference frequency components in the output are measured and reported in dBFS.

This is essentially the procedure specified in AES-17, except for a 1 dB reduction in signal level. The AES-17 directive to perform IMD measurements at full scale is dangerous in that clipping can occur with minor changes in level resulting in unfairly elevated distortion values. This is avoided by using the -1 dBFS level specified here.

Low Frequency Intermodulation Distortion

Low frequency intermodulation distortion (LF IMD) is another test of converter distortion or the amount of "junk" added to a clean audio signal. It uses two widely spaced sinewaves, one high frequency and one low frequency. The modulation induced on the high one by the low one is measured. As with the high frequency intermodulation measurement it is possible to assess nonlinearities at frequencies close to the high frequency bandwidth limit of the converter. Unlike the other test, this looks for low frequency converter limitations as can occur with inadequately stiff reference voltage regulation and filtering.

The converter is driven with two sinewaves, one low frequency (41 kHz) and one high frequency (7993 Hz). The low frequency sine amplitude is 4 times that of the high frequency sine and their combined peak-peak amplitude reaches 1 dB below the full the scale input amplitude. The output spectrum is provided graphically. The sum of second- and third-order difference frequency components in the output are measured and reported in dBFS.

This is essentially the procedure specified in AES-17, except for a 1 dB reduction in signal level. The AES-17 directive to perform IMD measurements at full scale is dangerous in that clipping can occur with minor changes in level resulting in unfairly elevated distortion values. This is avoided by using the –1 dBFS level specified here.

Amplitude Linearity

An amplitude linearity test examines the behavior of converters with varying input signal level. It is particularly sensitive to modulation of the background noise by the input signal and in showing inconsistent quantization behavior.

Called level-dependent logarithmic gain in AES-17, this measurement stimulates the converter with a 997 Hz sinewave of varying amplitude. The amplitude of the output sinewave is measured using a narrow bandpass filter to exclude noise, harmonics and spurious tones. The sinewave amplitude is swept from -5 dBFS to -115 dBFS and the deviation in the measured amplitude from the expected amplitude is determined. The linearity measurement differs from AES-17 in that the range is fixed, not dependent on the noise floor. This simplifies comparisons between converters. The result is expressed as a graph of this deviation as a function of input amplitude. In addition to this, the result should be expressed as a standard deviation value.

Spurious Aharmonic Signals

This measurement of spurious aharmonic signals looks at all components created in the output of the converter. The unit being tested is driven with a low distortion 997 Hz sinewave at -1 dBFS. The output spectrum is measured with a 32,768 point FFT. The full spectrum is graphed for informational purposes. For comparison, the largest aharmonic component is reported.

Alias Suppression

Alias suppression examines the ability of a converter to reject frequencies above one half the sample rate. If these are not eliminated they will appear in the output but at frequencies very different from what they had originally. This can result in strange tones and noises within the audio band that become a permanent, improper part of the recorded signal. This can be a serious problem when recording the output of analog tape recorders that leak bias signals into their outputs or when recording signals which include ultrasonic components.

The device is stimulated with a variable frequency sine wave at -10 dBFS. Beginning at half the sample rate, the frequency is continuously increased until it reaches 200 kHz. For a 48 kHz sample rate, the frequency is swept from 24 kHz to 200 kHz. For a 96 kHz sample rate, the frequency is swept from 48 kHz to 200 kHz. The rms amplitude at the converter output, increased by 10 dB, is graphed.

The difference from AES-17 is the elimination of variable frequencies based on a specified upper band edge frequency. This simplifies comparisons across converters. By starting at one half the sample rate, the AES-17 requirement for a notch filter is eliminated and the test becomes much simpler.

Cross-Talk

This measurement of cross-talk assesses how much the various channels in a multichannel converter interfere with each other. One channel is driven and the amount of that signal appearing in the other channel outputs is measured.

One channel of the converter under test is driven with a -1 dBFS variable frequency sinewave. The output of the other channels is passed through a narrow bandpass filter to assess its level, even close to the noise floor. This amplitude is expressed in dB relative to the sinewave output on the channel being driven. The measurement is performed at 20 Hz, 1 kHz and 20 kHz.

Cross-talk requirements are highly application dependent (i.e. The stringency of cross-talk is much higher for unrelated channels than related channels).

Common-Mode Rejection Ratio (CMRR)

If a signal is applied equally to both inputs of a device so that the differential input voltage is unaffected, the output should not be affected. Voltage that is common between either of the inputs and ground is called common-mode voltage. As this common voltage is varied, the perfect differential device's output voltage should hold absolutely steady (no change in output for any arbitrary change in common-mode input). In practice, however, changes in common mode voltage will produce changes in output; common-mode rejection ratio (CMRR) is the ratio of the common-mode gain to differential-mode gain. In simple terms, CMRR speaks to the ability of a device to reject noise and interference that is not part of the source signal. This noise and interference is typically the result of electromagnetic pickup in wiring between the source and the converter input.

The converter input is driven from a low impedance sinewave generator. The amplitude is adjusted to achieve -20 dBFS at the device output. The signal is removed, and the generator reconnected between the chassis ground and one side of the input. A 10 Ohm resistor is connected between this point and the other side of the input. If the input is asymmetrical, the generator is connected to the low side and the resistor to the high side. The output is measured through a bandpass filter at the sinewave frequency. The resulting rms value is reported relative to this -20 dBFS reference. The measurement is performed at 20 Hz, 1 kHz and 20 kHz.

This technique, and the 10 Ohm resistance value, corresponds to IEC 60268-3, which provides a newer method of measuring CMRR. It recognizes that rejection of interference is fundamentally limited by how a differential input deals with mismatches in the two sides of a source. Most sources are asymmetrical: balanced sources due to mismatches in the components comprising the two sides, and unbalanced sources due to the complete lack of source resistance on the low (or chassis) side. Previous CMRR tests tied the two halves of an input together and did not account for asymmetrical loading of the input.

Input Overload Behavior

Some converters behave erratically when their inputs are overloaded, either completely zeroing their output or swinging wildly between positive and negative full scale. This test quantifies the management of overloading by gradually increasing input level and looking at the distortion at the converters output.

The converter is driven with a low distortion sine wave whose amplitude is adjusted to yield -1 dBFS at the converter output. The amplitude is increased by 6 dB in 1 dB steps. The sine wave present in the output is removed with a notch filter and the rms amplitude of the remainder is measured.

This is the same basic approach used in AES-17 but finer amplitude steps are used to record more detail.

Clock and Jitter Test Methods and Metrics

Jitter is defined and described in an Audio Engineering Society Information Document pertaining to digital audio measurements, revised in 2011: *Jitter Performance Specifications*, AES-12id-2006 (r2011).[9] The introduction to this document begins with this statement: "Clocks tick at the heart of every digital audio product. Jitter on clocks that are applied to audio converters (analog-to-digital and digital-to-analog) can degrade audio performance." The document defines jitter as "the dynamic deviation of event instants in a stream or signal from their ideal positions in time, excluding modulation components below 10 Hz."

Jitter manifests itself in two places: in the sampling process (***sampling jitter***), and in the digital interface (***interface jitter***). When an ADC is only referencing its own sampling clock, the jitter that is present is referred to as ***intrinsic jitter***. ADCs may also reference an external sampling clock via digital interface, and the jitter present at the input to the ADC is referred to as interface jitter. Depending on the severity of the interface jitter and the design of the ADC, interface jitter can increase sampling jitter. The passing of jitter from an interface to sampling jitter is referred to as ***jitter transfe***r. The ability of a device to attenuate interface jitter and keep it from adding to sampling jitter is referred to as ***sync input jitter susceptibility***. The additive accrual of jitter through a chain of devices is called ***jitter accumulation*.**

TC-04 provides the following performance specifications addressing clocks and jitter:

- Internal Sample Clock Accuracy. For an A/D converter synchronized to its internal sample clock, frequency accuracy of the clock measured at the digital stream output will be better than ±25 ppm.
- External Synchronization. Where the A/D converter sample clock will be synchronized to an external reference signal, the A/D converter must react transparently to incoming sample rate variations ±0.2% of the nominal sample rate. The external synchronization circuit must reject incoming jitter so that the synchronized sample rate clock is free from artifacts and disturbances.
- Jitter. Interface jitter measured at A/D output <5 ns.

Our approach to assessing clocking and jitter take a slightly different approach to jitter and clocking, as outlined in the following sections of this document:

- Sync Input Jitter Susceptibility
- Jitter Transfer Gain
- Sync Input Lock Range

[9] http://www.aes.org/publications/standards/search.cfm?docID=57

Internal Sample Clock Accuracy was omitted based on the fact that the probability of inaccuracy to the extent of causing issues within a typical preservation setup using present-day ADCs is low. This parameter does not speak to the jitter of a clock, but rather small drifts from the sampling frequency that occur due to temperature changes and over time. Based on the quality of the converters included in this study there are no real practical implications to their sample clock accuracy specifications.

Sync Input Jitter Susceptibility

Converters which sync to an external reference signal become dependent to varying degrees on the cleanliness of that signal. This test looks at the ability of the converter to reject interference which may be present on the reference and consequently the impact of sync interface jitter on sampling jitter.

The converter input is driven with a -3 dBFS low distortion sinewave at 12 kHz. The reference input is driven with a signal whose phase is jittered with a 40 ns p-p sinewave whose frequency varies from 62.5 Hz to 8 kHz in octave steps. The output spectrum is measured at each step and the results overlaid. The measurements are repeated with a 997 Hz input to the converter.

This is equivalent to the procedure in AES-17 except that the device is assumed to be only an analog-to-digital converter. If a digital-to-analog function is included, it is not used in our testing. Measurements are made locking the converter through its reference input, not its D/A converter input. This simplification eases comparisons across the variety of devices being tested and reduces the number of permutations which would otherwise need to be tested. AES-17 also specifies that the jitter signal "is varied from 80 Hz to 20 kHz in octave steps." The range specified here goes from 62.5Hz to 8kHz. Incrementing by octaves starting at 80 Hz does not get to 20 kHz. Also, with a 12 kHz tone, sidebands from a 10 kHz modulation are about as high as can be seen. Consequently the frequency range was changed to begin and end on an IEC standard octave frequency. The upper end is set to a frequency that fits within the sideband limitations of the 12 kHz tone.

Jitter Transfer Gain

Jitter transfer gain is a metric that pertains to a converter locking to an external reference. This test analyzes the amount of interface jitter that persists from the sync input to through the digital output of the device. There is rarely enough effect to impact the ability of subsequent devices to lock to the resulting digital signal. However, if devices with poor jitter transfer behavior are cascaded the cumulative effect has been known to cause problems. Moreover, converter behavior in this test reveals limitations in the devices sync input design and gives insight to its ability to properly function in a more complex digital signal chain.

The reference input is driven with a signal whose phase is jittered by a 40 ns p-p sine-wave at frequencies from 62.5 Hz to 8 kHz in octave steps. The p-p jitter at the output is measured at each step. AES-17 specifies that the jitter signal “is varied from 80 Hz to 20 kHz in octave steps.” Incrementing by octaves starting at 80 Hz does not get to 20 kHz. For simplicity

sake, the jitter frequencies used here were chosen to be the same as the range used for jitter susceptibility measurements.

Sync Input Lock Range

Sync input lock range pertains to the risk that a converter will fail to lock to an external reference when there is a large difference between the external clock's sample rate and the converter's internal clock's sample rate. Large differences can cause problems with the converter achieving lock. There is an inherent tradeoff between a converters ability to lock to a wide deviation in reference frequency and its performance once locked.

The reference input is driven with a variable sample rate digital signal. The rate is varied from 48 kHz and the range over which the converter will lock is recorded. The reference should remain stable at each new frequency tested for at least 5 seconds before verifying lock.

Converters used to be expected to lock over a very wide range, typically up to 10% variation in sample rate. This stems from the desire to replace the "varispeed" function of analog tape recorders. This function is now implemented in digital processing devices and is no longer considered to be a requirement to address during signal capture. In this case a converter does not have to lock over as wide a range. Given the tradeoff on rejection of sync input jitter it is prudent to seriously consider the lock range required.

General Conditions

All measurements except Jitter Transfer Gain and Sync Input Lock Range are performed on all input channels. Significant differences are reported.

The measurements are performed at nominal line voltage +5% and -10% and any discrepancies are reported.

Each device under test is powered and operational for at least 30 minutes before measurements are performed.

Test Equipment

The test system is a collection of equipment from Qualis Test Systems, Audio Precision, Fluke and Tektronix, controlled by personal computer. In general, measurements were substantially above the test system residuals except when measuring the jitter and sideband performance for one of the ADCs.

The ambient temperature was maintained between 70 and 74 F for all tests. The line voltage was controlled with a General Radio variac to allow spot testing at voltage extremes and to ensure consistent line voltage for the entire suite of measurements.

Device Testing and Specification Refinement

This section compares measurements across the five devices tested. Objective performance measures produced quite different results on the five converters tested. The key results have been collected into tables to ease comparisons between converters.

Where IASA TC-04 limits exist they are included in the comparison tables. When a converter fails the performance limit the data is shown in red.

Frequency Response

All the converters tested passed the IASA TC-04 specification limits at 48 kHz except the defective channel on device 3, although that device and one other were very near the IASA "fail" point. One of these two also did not pass the 20 kHz response limit at the 96 kHz sample rate.

48 kHz Sample Rate

Frequency	IASA Limit	Device 1		Device 2		Device 3		Device 4		Device 5	
		Left	Right	Left	Right	Left	Right	Left	Right	Left	Right
20 - 20k Hz	+/- 0.1 dB	-0.03	+0.01	-0.03	+0.01	-0.10	-0.75	0.0	0.0	-0.09	-0.09

96kHz Sample Rate

Frequency	IASA Limit	Device 1		Device 2		Device 3		Device 4		Device 5	
		Left	Right	Left	Right	Left	Right	Left	Right	Left	Right
20 – 20k Hz	+/- 0.1 dB	-0.02	+0.00	-0.02	+0.00	-0.10	-0.75	0.0	0.0	-0.13	-0.13
20k – 40k Hz	+/- 0.3 dB	-0.02	+0.05	-0.02	+0.05	-0.40	-0.75	+0.01	+0.01	-0.19	-0.19

Based on our findings we recommend the following performance specifications:

Sample Rate	Frequency	Limit
48kHz	20 – 20k Hz	+/- 0.1 dB
96kHz	20 – 20k Hz	+/- 0.1 dB
96kHz	20k - 40k Hz	+/- 0.5 dB

The amplitude tolerance change from +/-0.3 dB to +/-0.5 dB for the range 20kHz to 40kHz accommodates antialias filters with lower echoes and gentler phase behavior. It accommodates designs that use wide transition bands (for instance between 30kHz and 40kHz) to reduce the time-domain effects of a sharp filter, without practical negative implications.

THD+N

Components inside the converter often approach their operating limits as signals reach the device's maximum input level. Consequently distortion tends to dominate performance at levels very close to full scale. When handling high frequency signals these components may have difficulty keeping up with the high rate of change of the signal. This can cause distortion to rise at higher frequencies. Similarly, inadequately stiff power supplies or thermal effects can cause the converter to have issues handling very slowly changing signals. This manifests itself as increased low frequency distortion. The result is that the -1 dBFS distortion measurements at the

three frequencies tested give a good picture of these issues. Note the performance of Device 2 and Device 4 at the higher amplitude in the table below.

48kHz Sample Rate Unweighted

Freq	Level	IASA Limit	Device 1		Device 2		Device 3		Device 4		Device 5	
Hz	dBFS		Left	Right	Left	Right	Left	Right	Left	Right	Left	Right
41	-1		-102.4	-106.3	-104.4	-104.3	-104.7	-102.6	-107.5	-106.9	-94.2	-94.7
997	-1	-105	-102.7	-106.0	-105.3	-105.5	-105.3	-105.6	-111.2	-110.5	-95.2	-96.4
6597	-1		-101.8	-104.7	-101.3	-100.7	-106.6	-106.3	-105.1	-105.4	-92.6	-93.3
41	-10		-99.5	-99.9	-99.9	-99.9	-106.3	-106.1	-103.5	-101.9	-95.9	-96.0
997	-10		-99.7	-100.1	-99.9	-99.9	-106.6	-106.3	-103.9	-102.7	-95.8	-96.2
6597	-10		-100.4	-100.7	-100.6	-100.1	-106.5	-106.2	-104.0	-102.6	-95.6	-96.0
41	-20		-91.4	-91.5	-91.0	-90.8	-98.0	-97.5	-94.8	-93.6	-89.2	-89.7
997	-20	-95	-91.6	-91.2	-91.0	-90.8	-98.1	-97.8	-95.3	-93.8	-89.6	-89.8
6597	-20		-91.6	-91.6	-91.7	-91.4	-98.4	-98.5	-95.7	-93.4	-90.1	-90.3
41	-60		-49.5	-49.8	-49.9	-49.6	-56.9	-56.4	-54.1	-52.7	-49.0	-49.3
997	-60		-50.8	-50.5	-49.9	-50.1	-57.2	-57.2	-54.2	-53.4	-49.3	-49.3
6597	-60		-51.1	-51.3	-50.4	-50.5	-57.5	-57.1	-54.4	-52.6	-46.2	-46.3

96kHz Sample Rate Unweighted

Freq	Level	IASA Limit	Device 1		Device 2		Device 3		Device 4		Device 5	
Hz	dBFS		Left	Right	Left	Right	Left	Right	Left	Right	Left	Right
41	-1		-101.9	-102.9	-104.4	-104.3	-104.6	-102.5	-107.4	-107.0	-93.4	-93.7
997	-1	-105	-101.5	-102.6	-105.3	-105.5	-105.5	-105.9	-110.6	-110.3	-94.5	-95.3
6597	-1		-97.8	-97.3	-101.3	-100.7	-106.8	-106.5	-105.0	-105.3	-92.1	-92.8
41	-10		-98.5	-99.0	-99.9	-99.9	-106.3	-106.1	-103.8	-103.1	-94.7	-95.0
997	-10		-98.1	-99.0	-99.9	-99.9	-106.5	-106.6	-103.7	-103.0	-94.9	-95.3
6597	-10		-98.5	-98.2	-100.6	-100.1	-106.4	-106.7	-103.9	-102.9	-94.9	-95.1
41	-20		-90.6	-90.5	-95.0	-94.1	-97.9	-97.1	-94.9	-94.1	-88.7	-88.7
997	-20	-95	-90.2	-90.5	-95.0	-94.2	-97.9	-97.4	-95.0	-94.2	-88.9	-89.2
6597	-20		-90.6	-90.2	-95.3	-94.4	-98.4	-98.3	-95.3	-94.4	-89.3	-89.7
41	-60		-47.7	-47.6	-49.9	-49.6	-56.9	-56.7	-54.1	-53.0	-49.0	-49.3
997	-60	-50	-49.9	-49.6	-49.9	-50.1	-56.8	-56.8	-54.1	-53.3	-49.2	-49.2
6597	-60		-50.0	-50.0	-50.4	-50.5	-57.7	-57.4	-54.7	-53.4	-49.7	-50.1

The frequency and level combinations highlighted in grey could be removed from the performance tests with no loss of completeness. Their presence serves mainly to observe the more important differences at the higher input levels.

Based on our findings we recommend the following performance specification:

Freq	Level	Limit (unweighted)
Hz	dBFS	
41	-1	-100
997	-1	-100
6597	-1	-100
997	-10	-100
997	-20	-90
997	-60	-50

Additional tests at lower amplitudes will demonstrate the way noise and distortion trade-off with each other. These rarely show frequency dependence as the noise begins to dominate the overall results. Whereas the IASA TC-04 specification provides reference points at -1dBFS and -20dBFS, we recommend two additional reference points be placed at -10dBFS, using a limit of -100dB unweighted, and -60dBFS, using a limit of -50dB. In addition to this, we recommend that performance specification limits be set for 41Hz and 6597 Hz in addition to 997Hz at the -1 dBFS amplitude. Implicit in this is the addition of these reference signals to the test method, following the same protocol as specified with the 997Hz signal. Based on our findings, we believe that these added data points will provide a more accurate reporting on the relevant THD+N characteristics of a given ADC.

Dynamic Range (Signal to Noise)

All converters except Device 3 failed the IASA TC04 limits.

	IASA Limit	Device 1		Device 2		Device 3		Device 4		Device 5	
		Left	Right	Left	Right	Left	Right	Left	Right	Left	Right
Unweighted	-115 dB	110.8	110.5	109.9	110.1	117.2	117.2	114.2	113.4	105.7	105.7
A weighted	-117 dB	113.1	113.4	112.4	112.3	119.4	119.7	116.7	116.3	108.6	108.6

Based on our findings we recommend the following performance specifications:

	Limit
Unweighted	-110 dB
A weighted	-112 dB

The failure of four of the five units suggested strongly that the IASA specification was too stringent. Relaxing the specification to the suggested values alleviates this issue while maintaining a level of stringency that we believe is appropriate for the intended application.

Cross-Talk

There is no IASA specification for cross-talk. We added cross-talk as a proposed performance specification with its own test method because of its strong implications to maintaining the integrity of the original recording. The performance specification required for cross-talk is highly dependent on the application. We believe that the varied applications in a preservation context mean that it is appropriate to use this somewhat demanding specification.

Frequency	Device 1		Device 2		Device 3*		Device 4		Device 5	
20 Hz	-131.3	-128.3	-162.2	-146.6			-129.9	-125.1	-103.9	-102.3
1k Hz	-111.7	-110.7	-133.6	-134.8			-137.4	-132.3	-109.3	-107.0
20 k Hz	-106.8	-110.7	-118.9	-116.1			-117.0	-120.0	-93.0	-92.3

Note: Results for Device 3 were unintentionally omitted.

The results demonstrate a great degree of variation in the performance of different converters, confirming the value of this performance parameter.. Based on our findings we recommend the following specification:

Frequency	Limit
20 Hz	-120 dB
1k Hz	-120 dB
20 k Hz	-110 dB

We believe that the chosen limits are reasonable points of delineation separating the poorer-performing from the better-performing devices while maintaining an appropriate level of stringency. The proposed amplitude curve across the frequency range places frequencies that are predominant in the range of human hearing 10 dB beneath the noise floor. This limit is more stringent than the dynamic range limit based since dynamic range is based on a wideband performance measure while cross-talk is based on sinewave leakage from one channel to another. A typical human observer is able to detect a tone and other information-carrying signals (e.g. speech, music) even at levels below the noise floor.

CMRR

There is no IASA specification for CMRR. It has been added as a proposed performance specification based on the fact that it indicates the ability of a device to reject noise that is not part of the incoming source signal, and the implications of this in the context of preservation. Higher dB values indicate better noise rejection.

Frequency	Device 1		Device 2		Device 3		Device 4		Device 5	
20 Hz	63.6	62.7	49.6	50.0	74.5	5.8	92.5	98.2	46.4	50.7
1k Hz	63.4	62.6	49.5	49.9	74.3	36.8	92.0	95.8	46.1	50.8
20 k Hz	56.8	54.0	49.4	49.8	75.9	55.4	68.9	72.8	46.1	50.8

Based on our findings, we recommend the following performance specification:

Frequency	Limit
60 Hz	70 dB
1k Hz	70 dB
20 k Hz	50 dB

Common mode interference is often due to power line issues making performance at low frequencies at least as important as mid band performance. Although the test was performed using a 20Hz it was decided to shift this to 60Hz.

The limits that have been set are based on analysis of the results and have been chosen to provide a specification that is simultaneously stringent and reasonable.

Intermodulation Distortion

As mentioned previously, testing of both low frequency and high frequency intermodulation distortion occurred. Typically only the "sum" value is reported in performance specifications. Here we have reported the individual values in addition to the sum. In the case of the LF IMD test we have reported an additional metric labeled "integrated". This is an addition to the test method discussed earlier in this report, and provides the results using a classic SMPTE IMD analyzer.

LF IMD

All of the tested units would pass the proposed specification if it is implemented using spectrum analysis. If an analyzer that integrates sideband noise and distortion across the 40 Hz to 500 Hz range (a classic SMPTE IMD analyzer) were used, then one of the devices would fail. The rows highlighted in grey are primarily for informational purposes.

	IASA Limit	Device 1		Device 2		Device 3		Device 4		Device 5	
2nd		-103.0	-116.1	-119.4	-111.3	-112.9	-116.7	-110.4	-110.2	-93.9	-97.1
3rd	-	-108.7	-113.4	-99.2	-99.1	-101.8	-101.1	-107.1	-107.3	-99.3	-97.7
sum	-90 dB	-102.0	-111.5	-99.2	-98.8	-101.5	-101.0	-105.4	-105.5	-92.8	-94.4
integrated		-95.1	-102.1	-94.8	-94.3	-94.9	-95.4	-102.9	-102.6	-88.3	-90.5

HF IMD

All of the tested units pass the proposed limit, although one is close.

	IASA Limit	Device 1		Device 2		Device 3		Device 4		Device 5	
2nd		-105.7	-129.0	-137.9	-117.3	-115.8	<-140	<-140	<-140	-94.3	-97.5
3rd		-113.3	-112.4	-106.3	-105.5	-112.1	-111.9	-105.2	-105.5	-93.3	-93.2
sum	-90 dB	-105.0	-112.3	-106.3	-105.2	-110.6	-111.9	-105.2	-105.5	-90.8	-91.8

Based on our findings we recommend performing both Low Frequency and High Frequency tests, and reporting associated performance specifications:

Frequency	Limit
LF sum	-100 dB
HF sum	-105 dB

We propose tightening the IASA specification based on analysis of the results in order to provide a specification that is simultaneously stringent and reasonable. Furthermore, we recommend explicitly reporting of this specification as the ***sum*** measurement, since we have seen that manufacturers vary in their reporting of ***sum*** and ***integrated*** IMD measurements.

Amplitude Linearity

There are challenges in condensing the graphical results of this measurement down to single a numeric metric that may be compared to limits. The original IASA range from -115 dBFS to -5 dBFS is too wide and encounters large deviations near the noise floor which do not represent true amplitude linearity issues. Therefore we recommend changing this range to -105 dBFS to -5 dBFS. The peak deviation specification in the IASA document also provides some challenges in fairly representing converter differences. A single errant point can set the maximum positive or negative deviation without regard for how well behaved the remainder of the curve may be. Therefore we recommend using a standard deviation specification across the range of interest. This is included in the table below. All deviations noted are the largest positive or negative change from one point to another on the same curve.

	IASA Limit	Device 1		Device 2		Device 3		Device 4		Device 5	
Max + dev. -105 to -5	+0.5 dB	+0.05	+0.05	+0.12	+0.09	+0.02	+0.2	+0.12	+0.8	+0.1	+0.16
Max – dev. -105 to -5	-0.5 dB	-0.22	-0.10	-0.13	-0.08	-0.3	-0.2	-0.6	-0.6	-0.27	-0.07
Std. Dev.-105 to -5		0.008	0.038	0.114	0.096	0.020	0.182	0.023	0.035	0.046	0.019

Based on our findings and the discussion above we recommend the following specifications:

	Limit
Standard Deviation	0.05 dB

As discussed above, a change to analyzing and reporting standard deviation is recommended. The limit was selected based on analysis of the results and selecting a reasonable point of delineation.

Spurious Aharmonic Signals

	IASA Limit	Device 1		Device 2		Device 3		Device 4		Device 5	
60/180/300 Hz	< -130	-100.1	-100.1	<-100	<-100	-129.7	-129.7	<-103	<-103	<-130	<-130
120/240 Hz	< -130	-118.2	-118.2	<-100	<-100	-123.2	-123.2	<-103	<-103	<-129	<-129

Based on our findings we recommend loosening the IASA specification as follows:

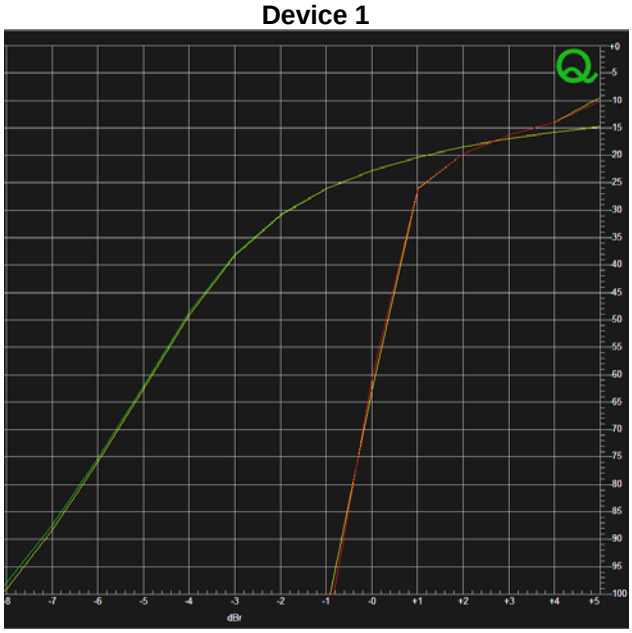
Frequency	Limit
> 50Hz	-100

The limit was set based on the results and establishing a more realistic specification.

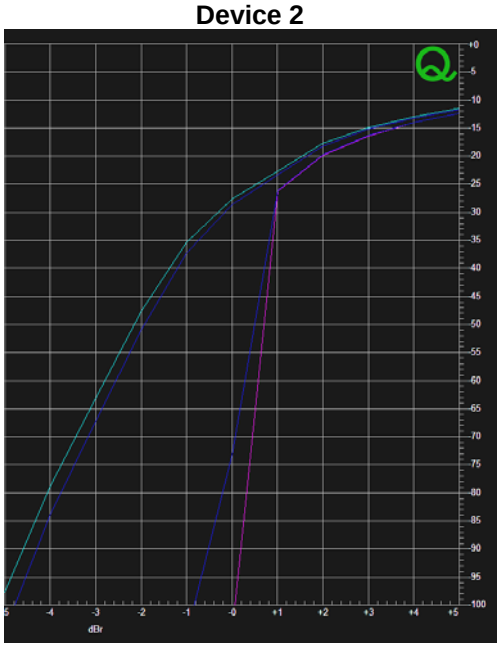
Input Overload Behavior

A proper numeric method of comparing overload behavior is still under development by AES committee SC-02-01. The converters tested all exhibited reasonable behavior when driven into overload. The measurement graphs are reproduced below.

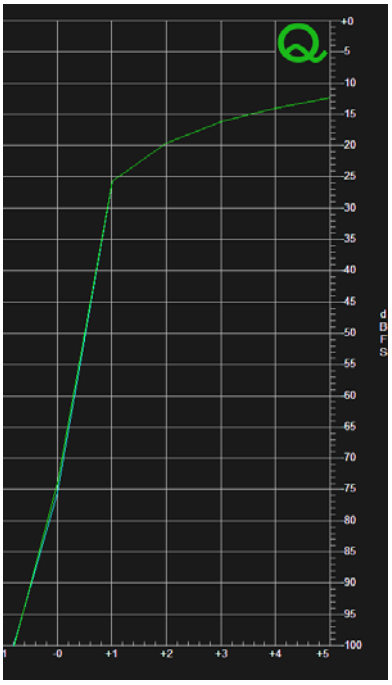
Device 1



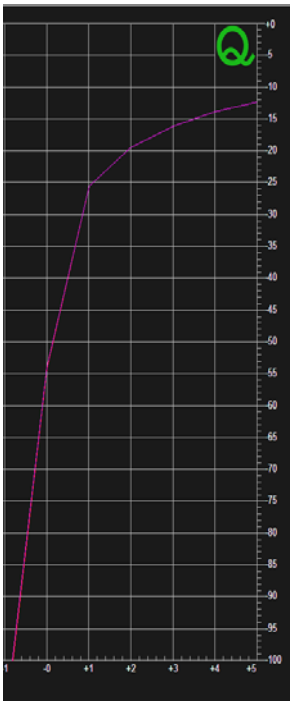
Device 2



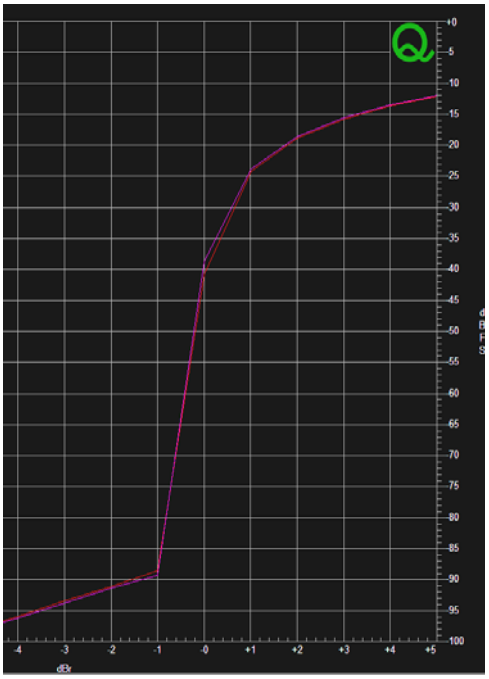
Device 3



Device 4



Device 5



Two of the professional units offer a special clipping management (limiter) functionality that can be turned off; we made two input overload measurements for each of these units, with the function turned off and turned on. Where the graphs above show two sets of curves (Device 1 & 2), one was made with the limiter function engaged and one with it off. The gradual rise, smooth curve, trace is with the limiter engaged. The result is gradually increasing distortion as signals approach full scale instead of an abrupt rise as full scale is reached. Due to time limitations, the effect on other measurements was not examined, but it is anticipated that it would result in significant differences in distortion and linearity performance.

There is no recommendation at this time for inclusion of this test method or a performance specification.

Alias Suppression

There is no specification for alias suppression in IASA TC-04. The results below identify the lowest frequency at which the alias component was equal to or greater in amplitude than all other alias components across the frequency range tested. Amplitude is expressed relative to the stimulus amplitude in dB.

SR	Device 1		Device 2		Device 3		Device 4		Device 5	
48 kHz	24 kHz	-96	27.5 kHz	-73	26.0 kHz	-98	27.7 kHz	-82	26.5 kHz	-88
96 kHz	24 kHz	-93	63 kHz	-72	51.9 kHz	-98	63.8 kHz	-80	53 kHz	-89

Based on our findings we recommend the following specifications:

SR	Limit
48 kHz	-80 dB
96 kHz	-80 dB

The proposed limits are based on analysis of the results and a determination of what represented a stringent yet reasonable specification.

Sync Input Jitter Susceptibility

There is no IASA performance specification for this parameter. Based on the implications for the common scenario of a converter referencing external synchronization, we believe that this metric is important. The jitter susceptibility of device 3 was extremely low, very near the limits of the measurement system. Not only was it highly resistant to jitter on its reference input but it introduced very little sideband noise on the test signal. Results are expressed as dBFS for each octave step.

12 kHz

Frequency	Device 1	Device 2	Device 3	Device 4	Device 5
8 kHz	-120.4	-129.4	-142.7	-141.1	-117.1
4 kHz	-108.4	-115.4	-138.2	-135.9	-50.3
2 kHz	-94.1	-101.7	-137.7	-133.7	-44.0
1 kHz	-79.6	-86.3	-122.5	-122.9	-99.3
500 Hz	-63.5	-75.3	-125.4	-108.7	-93.3
250 Hz	-55.4	-69.6	-117.5	-90.7	-87.4
125 Hz	-56.7	-63.3	-118.3	-70.5	-81.1
63 Hz	-56.3	-59.6	-118.3	-63.2	-75.0

997 Hz

Frequency	Device 1	Device 2	Device 3	Device 4	Device 5
500 Hz	-100.2	-96.6	-138.2	-129.2	-114.3
250 Hz	-76.2	-87.0	-139.5	-111.6	-108.4
125 Hz	-77.3	-80.0	-132.5	-92.2	-102.5
63 Hz	-77.9	-76.3	-122.1	-84.8	-96.7

Based on our findings, we recommend the following specifications:

12 kHz

Frequency	Limit
8 kHz	-130 dB
4 kHz	-120 dB
2 kHz	-120 dB
1 kHz	-120 dB
500 Hz	-100 dB
250 Hz	-90 dB
125 Hz	-70 dB
63 Hz	-60 dB

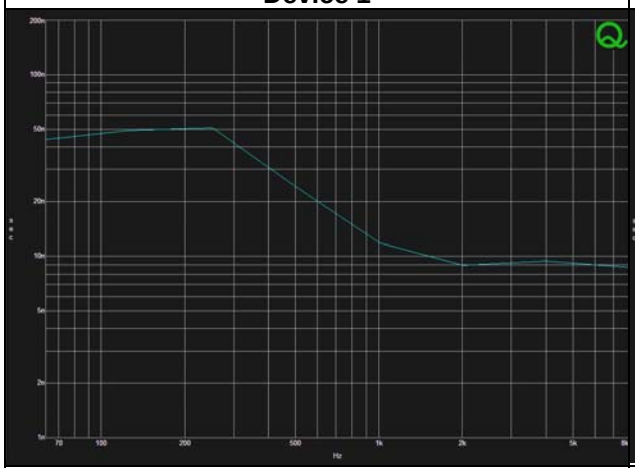
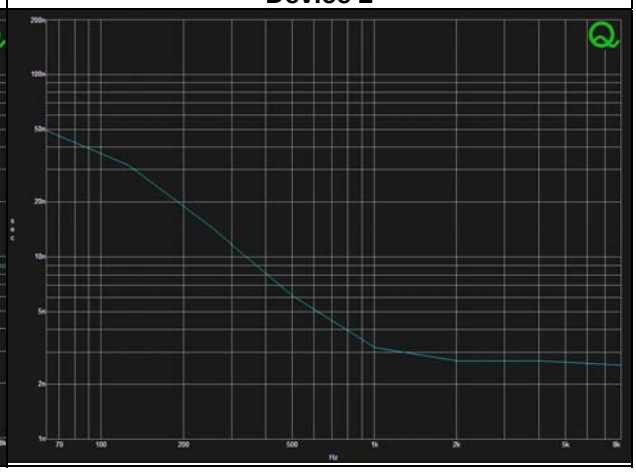
997 Hz

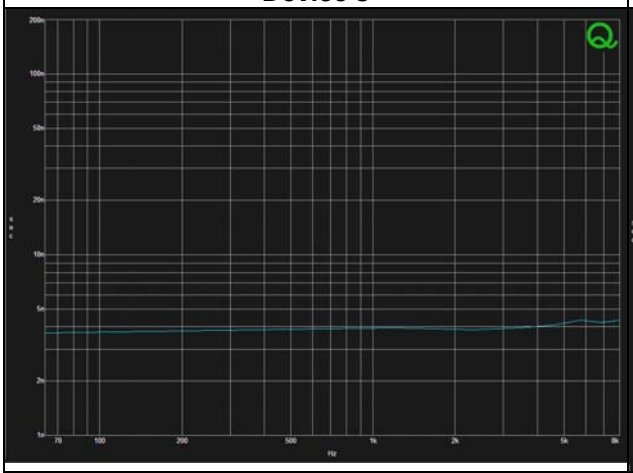
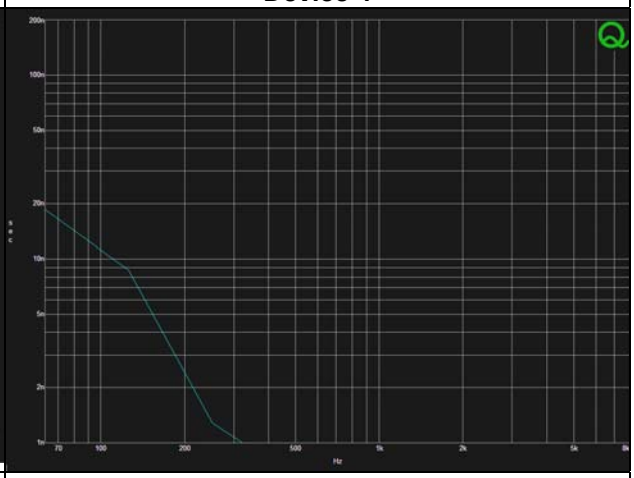
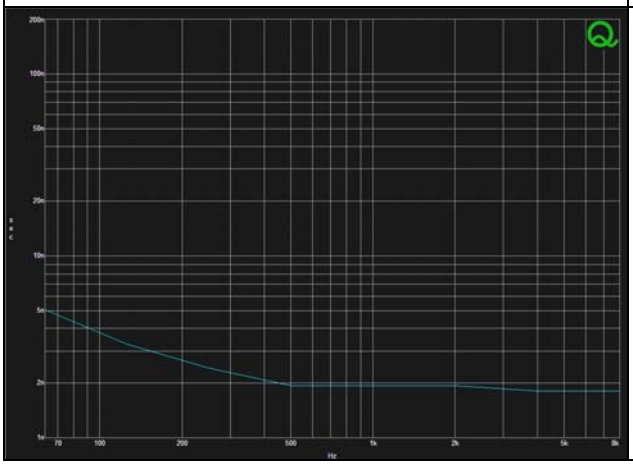
Frequency	Limit
500 Hz	-110 dB
250 Hz	-100 dB
125 Hz	-90 dB
63 Hz	-80 dB

The referenced frequencies are implicit in the test method. The limits are based on analysis of the results and a determination of what was both stringent and reasonable.

Jitter Transfer Gain

This specification is a variation on IASA's *Jitter* performance specification. This test assesses *jitter gain* as a result of jitter referenced against the jitter at the sync input. The addition of this reference point provides a meaningful look into the implications to the audio signal. Measuring interface jitter alone does not give an indication of the impact to audio performance. Interface jitter and sampling jitter are two distinct metrics and measuring the former does not provide a direct link to assessing the latter.

Device 1	Device 2
	

Device 3	Device 4
	
Device 5	
	

Based on our findings we recommend the following specifications:

Limit
< 20ns p-p

The limit was chosen based on assessing the range found within the results and making a determination of what was simultaneously stringent yet reasonable.

Sync Input Lock Range

	IASA Limit	Device 1		Device 2		Device 3		Device 4		Device 5	
Lock	2%	<-1%	>+1%	<-1%	>+1%	-0.016%	+0.014%	<-1%	>+1%	<-1%	>+1%
Acquire	2%	<-1%	>+1%	<-1%	>+1%	-0.012%	+0.009%	<-1%	>+1%	<-1%	>+1%

The tradeoff between jitter rejection and Sync Input Lock Range showed dramatically. However, monitoring THD+N and Spurious Aharmonic Signals demonstrated that all units performed as well when operating at the limits of their lock range as they did when locked to a nominally correct signal. In addition to this, 2% tolerance is much wider than necessary and represents locking to a grossly inaccurate reference. There is very little practical application that justifies such a wide tolerance. Furthermore, there is a direct tradeoff with jitter rejection as evidenced by the excellent rejection performance of device #3 compared to all the other units. The lack of practical application and the implicit worsening of jitter rejection does not justify specifying a wider lock range. Based on our findings, we recommend omitting this test method and performance specification.

Summary and Conclusions

We felt that the testing process generally validated our view that there is a need for a core test method and associated set of performance specifications. Although this was not an exercise in testing ADCs - we did not, for example, run the tests on multiple samples of each device - we saw that in this group of five, two were very good performers, two were in the middle, and one was noticeably worse. The devices tend to excel and fall short on different performance facets, no doubt revealing the design tradeoffs that face all manufacturers.

Based on findings of this study, we recommended some changes to the IASA Performance Specifications and the associated test methods. The final recommended set of test methods and performance specifications is provided in Appendix A.

Appendix A: Recommended ADC Performance Guideline

Test Method Name	**Frequency Response**
IASA Performance Specification Name	Frequency Response
IASA Specification	For an A/D sampling frequency of 48 kHz, the measured frequency response will be better than ± 0.1 dB for the range 20 Hz to 20 kHz. For an A/D sampling frequency of 96 kHz, the measured frequency response will be better than ± 0.1 dB for the range 20Hz to 20 kHz, and ± 0.3 dB for the range 20 kHz to 40 kHz. For an A/D sampling frequency of 192 kHz, the frequency response will be better than ± 0.1 dB for the range 20Hz to 20 kHz, and ± 0.3 dB from 20 kHz to 50 kHz (reference audio signal = 997 Hz, amplitude -20 dB FS).
Recommended Test Method	According to AES-17: Frequency response shall be measured at –20 dBFS with a sinewave whose frequency varies from 10 Hz to 50 kHz in steps no larger than 10 per octave.
Recommended Performance Specification	

Sample Rate	Frequency	Limit
48kHz	20 – 20k Hz	+/- 0.1 dB
96kHz	20 – 20k Hz	+/- 0.1 dB
96kHz	20k - 40k Hz	+/- 0.5 dB

Test Method Name	**Total Harmonic Distortion + Noise (THD+N)**
IASA Performance Specification Name	Total Harmonic Distortion + Noise (THD+N)
IASA Specification	With signal 997 Hz at -1 dB FS, the A/D converter THD+N will be less than -105 dB unweighted, -107 dB A-weighted, 20 Hz to 20 kHz bandwidth limited. With signal 997 Hz at -20 dB FS, the A/D converter THD+N will be less than -95 dB unweighted, -97 dB A-weighted, 20 Hz to 20 kHz bandwidth limited.
Recommended Test Method	Based on AES-17: The EUT shall be stimulated with a low distortion sine wave. The test signal present in the output shall be removed with a notch filter and bandwidth limited from 20 Hz to 20 kHz. The RMS amplitude is reported as a ratio to the RMS amplitude of the unfiltered signal. The measurement should be performed at the following amplitude and frequency combinations: -1.0 dBFS at 41 Hz, 997 Hz and 6597 Hz, –10 dBFS at 997 Hz, and -20 dBFS at 997 Hz, and -60 dBFS at 997 Hz.
Recommended Performance Specification	

Freq	Level	Limit (unweighted)
Hz	dBFS	
41	-1	-100
997	-1	-100
6597	-1	-100
997	-10	-100
997	-20	-90
997	-60	-50

Test Method Name	**Dynamic Range (Signal to Noise)**
IASA Performance Specification Name	Dynamic Range (Signal to Noise)
IASA Specification	The A/D converter will have a dynamic range of not less than 115 dB unweighted, 117 dB A-weighted. (Measured as THD+N relative to 0 dB FS, bandwidth limited 20 Hz to 20 kHz, stimulus signal 997 Hz at -60 dB FS).
Recommended Test Method	Based on AES-17: The measurement is the ratio of the full-scale amplitude to the weighted r.m.s. noise and distortion, expressed in dB, in the presence of signal. It includes all harmonic, inharmonic, and noise components. The test signal shall be a 997-Hz sine wave producing – 60 dBFS at the EUT output. Any 997-Hz test signal present in the output is removed by means of a standard notch filter. The remaining noise is filtered with an A weighting filter limited to 20 kHz. The results shall be reported as unweighted and A-weighted in dBFS.
Recommended Performance Specification	**Weighting** / **Limit** Unweighted / -110 dB A weighted / -112 dB

Test Method Name	**Cross-Talk**
IASA Performance Specification Name	Not present
IASA Specification	Not Applicable
Recommended Test Method	One channel of the EUT is driven with a -1 dBFS sinewave and the maximum amplitude of this frequency appearing in any other channel is noted. The measurement is repeated for each input channel and the maximum amplitude for all channels is determined. This amplitude, expressed in dBFS, is increased by 1 dB and reported. The measurement shall be performed at frequencies of 20 Hz, 1 kHz and 20 kHz.
Recommended Performance Specification	**Frequency** / **Limit** 20 Hz / -110 dB 1k Hz / -110 dB 20 k Hz / -105 dB

Test Method Name	**Common-Mode Rejection Ratio (CMRR)**
IASA Performance Specification Name	Not present
IASA Specification	Not Applicable
Recommended Test Method	The input shall be driven from a sinewave generator whose output impedance is less than 100 Ohms. The amplitude is adjusted to achieve -20 dBFS at the EUT output. The signal is removed, and the generator reconnected between the chassis ground and one side of the input. A 600 Ohm resistor is connected between this point and the other side of the input. If the input is asymmetrical, the generator should be connected to the low side and the resistor to the high side. The output should be measured through a bandpass filter at the sinewave frequency. The resulting RMS value, measured in dBFS, is increased by 20 dB and reported as a dB (not dBFS) value. The measurement should be performed at 60 Hz, 1 kHz and 20 kHz.
Recommended Performance Specification	**Frequency** / **Limit** 60 Hz / 70 dB 1k Hz / 70 dB 20 k Hz / 50 dB

Test Method Name	**Low Frequency Intermodulation Distortion (LF IMD)**
IASA Performance Specification Name	Intermodulation Distortion (IMD)
IASA Specification	The A/D converter IMD will not exceed -90 dB. (AES17/SMPTE/DIN twin-tone test sequences, combined tones equivalent to a single sine wave at full scale amplitude).
Recommended Test Method	Based on AES-17: IM measurements shall be performed with a twin tone signal with a peak amplitude of -1.0 dBFS. The lrms sum of second- and third-order difference frequency components in the output are measured and reported in dBFS. The test frequencies shall be 41 Hz and 7993 Hz in a 4:1 amplitude ratio.
Recommended Performance Specification	**Frequency** / **Limit** LF sum / -100 dB

Test Method Name	**High Frequency Intermodulation Distortion (HF IMD)**
IASA Performance Specification Name	Intermodulation Distortion (IMD)
IASA Specification	The A/D converter IMD will not exceed -90 dB. (AES17/SMPTE/DIN twin-tone test sequences, combined tones equivalent to a single sine wave at full scale amplitude).
Recommended Test Method	Based on AES-17: IM measurements shall be performed with a twin tone signal with a peak amplitude of -1.0 dBFS. The lrms sum of second- and third-order difference frequency components in the output are measured and reported in dBFS. The test frequencies shall be 20 kHz and 18 kHz in a 1:1 amplitude ratio.
Recommended Performance Specification	**Frequency** / **Limit** HF sum / -105 dB

Test Method Name	**Amplitude Linearity**
IASA Performance Specification Name	Amplitude Linearity
IASA Specification	The A/D converter will exhibit amplitude gain linearity of ± 0.5 dB within the range -120 dB FS to 0 dB FS. (997 Hz sinusoidal stimuli).
Recommended Test Method	Based on AES-17: Level-dependent logarithmic gain is measured at 997 Hz from -5 dBFS to -115 dBFS and reported as standard deviation value in dB.
Recommended Performance Specification	**Limit** Standard Deviation / 0.05 dB

Test Method Name	**Spurious Aharmonic Signals**
IASA Performance Specification Name	Spurious Aharmonic Signals
IASA Specification	Better than -130 dB FS with stimulus signal 997 Hz at -1 dBFS
Recommended Test Method	A 997 Hz sinewave shall be applied at -1 dBFS. The output spectrum shall be measued with an 32,768 point FFT. The largest inharmonic component is reported in dBFS.
Recommended Performance Specification	**Frequency** / **Limit** > 50Hz / -100

Test Method Name	**Alias Rejection**
IASA Performance Specification Name	Not present
IASA Specification	Not applicable
Recommended Test Method	Based on AES-17 and IEC 61606-3: The device is stimulated with a variable frequency sine wave at -10 dBFS. Beginning at half the sample rate, the frequency is continuously increased until it reaches 200 kHz. For a 48 kHz sample rate, the frequency is swept from 24 kHz to 200 kHz. For a 96 kHz sample rate, the frequency is swept from 48 kHz to 200 kHz. The rms amplitude at the converter output, increased by 10 dB, is graphed. Results are reported as the lowest frequency at which the alias component was equal to or greater in amplitude than all other alias components across the frequency range tested. Amplitude is expressed relative to the stimulus amplitude in dB.
Recommended Performance Specification	**SR** / **Limit** 48 kHz / -80 96 kHz / -80

Test Method Name	**Sync Input Jitter Susceptibility**
IASA Performance Specification Name	Not present
IASA Specification	Not applicable
Recommended Test Method	Based on AES-17: The converter input is driven with a -3 dBFS low distortion sinewave at 12 kHz. The reference input is driven with a signal whose phase is jittered with a 40 ns p-p sine-wave whose frequency varies from 62.5 Hz to 8 kHz in octave steps. The output spectrum is measured at each step and the results overlaid. The measurements are repeated with a 997 Hz input to the converter. Results are expressed as dBFS for each octave step.

<table>
<tr><td>Recommended Performance Specification</td><td>

12 kHz

Frequency	Limit
8 kHz	-130 dB
4 kHz	-120 dB
2 kHz	-120 dB
1 kHz	-120 dB
500 Hz	-100 dB
250 Hz	-90 dB
125 Hz	-70 dB
63 Hz	-60 dB

997 Hz

Frequency	Limit
500 Hz	-110 dB
250 Hz	-100 dB
125 Hz	-90 dB
63 Hz	-80 dB

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Test Method Name	**Jitter Transfer Gain**
IASA Performance Specification Name	Jitter (related but not equivalent)
IASA Specification	Interface jitter measured at A/D output <5ns (related but not equivalent)
Recommended Test Method	Based on AES-17: The reference input shall be driven with a signal whose phase is jittered with a 40 ns p-p sine-wave jitter signal whose frequency varies from 62.5 Hz to 8 kHz in octave steps. The p-p jitter at the output shall be measured at each step and the results shall be graphed. Results shall also report the maximum p-p jitter value in ns.
Recommended Performance Specification	**Limit** < 20ns p-p